1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Sully

M9 MLB
3/3/2006

DVT
(6.0.0)

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

Page (.csa)	Contents	Sync	Date
1	Table of Contents	N/A	N/A
2	System Block Diagram	(MASTER)	(MASTER)
3	Power Block Diagram	(MASTER)	(MASTER)
4	BOM Configuration	(MASTER)	(MASTER)
5	Functional / ICT Test	(MASTER)	(MASTER)
6	Signal Aliases	(M1_MLB)	(11/11/2005)
7	CPU 1 OF 2-FSB	M1_MLB	02/10/2006
8	CPU 2 OF 2-PWR/GND	M1_MLB	02/10/2006
9	CPU Decoupling & VID	M1_MLB	02/08/2006
10	CPU MISC1-TEMP SENSOR	M1_MLB	02/10/2006
11	CPU ITP700FLEX DEBUG	M1_MLB	02/10/2006
12	NB CPU Interface	M1_MLB	02/10/2006
13	NB PEG / Video Interfaces	M1_MLB	02/10/2006
14	NB Misc Interfaces	M1_MLB	02/10/2006
15	NB DDR2 Interfaces	M1_MLB	02/10/2006
16	NB Power 1	M1_MLB	02/10/2006
17	NB Power 2	M1_MLB	02/10/2006
18	NB Grounds	M1_MLB	02/10/2006
19	NB (GM) Decoupling	M1_MLB	02/08/2006
20	NB Config Straps	M1_MLB	02/10/2006
21	SB: 1 OF 4	M1_MLB	02/10/2006
22	SB: 2 of 4	M1_MLB	02/10/2006
23	SB: 3 OF 4	M1_MLB	02/10/2006
24	SB: 4 OF 4	M1_MLB	02/10/2006
25	SB Decoupling	M1_MLB	02/10/2006
26	SB Misc	M1_MLB	02/10/2006
27	M1 SMBus Connections	M1_MLB	01/04/2006
28	DDR2 SO-DIMM Connector A	M1_MLB	02/10/2006
29	DDR2 SO-DIMM Connector B	M1_MLB	02/10/2006
30	Memory Active Termination	(M1_MLB)	(11/07/2006)
31	Memory Vtt Supply	M1_MLB	02/10/2006
32	DDR2 VRef	M1_MLB	12/19/2005
33	CLOCKS	M1_MLB	02/10/2006
34	Clock Termination	M1_MLB	02/10/2006
37	Mobile Clocking	M1_MLB	02/10/2006
38	PATA Connector	M1_MLB	02/10/2006
39	FireWire Link (TSB83AA22)	(MASTER)	(MASTER)
40	FireWire PHY (TSB83AA22)	(MASTER)	(MASTER)
41	ETHERNET CONTROLLER	M1_MLB	02/10/2006
42	Ethernet Connector	M1_MLB	02/10/2006
43	Yukon Power Control	M1_MLB	02/10/2006
44	FW PHY Power Supply	(MASTER)	(MASTER)
45	FireWire Port Power	(M1_MLB)	(11/03/2005)
46	FireWire Ports	(MASTER)	(MASTER)
49	Internal USB Connections	M1_MLB	02/10/2006
52	External USB Connector	M1_MLB	02/10/2006
55	Left I/O Board Connector	(MASTER)	(MASTER)
56	Current & Thermal Sensors	(MASTER)	(MASTER)
57	PCI-E Connections	M1_MLB	02/10/2006
58	SMC	M1_MLB	02/10/2006
59	SMC Support	M1_MLB	02/10/2006
60	LPC+ Debug Connector	M1_MLB	02/10/2006
61	Thermal Sensors	M1_MLB	02/10/2006
62	Current & Voltage Sensing	M1_MLB	01/05/2006
63	SPI BOOTROM	M1_MLB	02/10/2006
64	ALS Support	M1_MLB	02/10/2006
65	Fan Connectors	M1_MLB	02/10/2006
66	Sudden Motion Sensor (SMS)	M1_MLB	02/10/2006
67	TPM	M1_MLB	02/10/2006
75	IMVP6 CPU VCore Regulator	M1_MLB	02/08/2006
76	5V / 1.5V Power Supply	M1_MLB	02/10/2006
77	2.5V & 1.2V Regulators	M1_MLB	02/10/2006
78	1.8V Supply	M1_MLB	02/10/2006
79	3.3V / 1.05V Power Supplies	M1_MLB	02/10/2006
80	3.3V G3Hot Supply & Power Control	M1_MLB	02/10/2006
81	Power Aliases	M1_MLB	12/19/2005
82	DC-In & Battery Connectors	(MASTER)	(MASTER)
83	PBus Supply & Batt. Charger	M1_LIO	12/19/2005
84	ATI M56 PCI-E	M1_MLB	02/10/2006
85	GPU (M56) Core Supplies	M1_MLB	02/10/2006
86	ATI M56 Core Power	M1_MLB	02/10/2006
87	ATI M56 Frame Buffer I/F	M1_MLB	02/10/2006
88	GPU Straps	M1_MLB	02/10/2006
89	GDDR3 Frame Buffer A	M1_MLB	02/10/2006
90	GDDR3 Frame Buffer B	M1_MLB	02/10/2006
91	ATI M56 GPIO/DVO/Misc	M1_MLB	02/10/2006
93	ATI M56 Video Interfaces	M1_MLB	02/10/2006
94	Internal Display Connectors	M1_MLB	01/09/2006
97	External Display Connector	M1_MLB	11/18/2005
98	M9 Specific Connectors	(MASTER)	(MASTER)
99	LVDS Interface Pull-downs	M1_MLB	12/19/2005
100	Revision History	(MASTER)	(MASTER)
101	Napa Platform Constraints	M1_MLB	02/10/2006
102	More System Constraints	M1_MLB	02/10/2006
103	M1 Spacing & Physical Constraints	M1_MLB	02/10/2006
104	M1 Net Properties	M1_MLB	02/10/2006

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7023	1	SCHEM,SULLY,M9	SCH	CRITICAL	
820-2023	1	PCBF,SULLY,FINAL,M9	PCB	CRITICAL	

DRAWING
TITLE=SULLY
ABBREV=DRAWING
LAST_MODIFIED=Fri Mar 3 17:59:45 2006

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER / DESIGN CK / ENG APPD / MFG APPD / QA APPD / DESIGNER / RELEASE / SCALE: NONE
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE: D

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TITLE
SCHEM,SULLY,M9

DRAWING NUMBER 051-7023 REV. 06
SHT 1 OF 86

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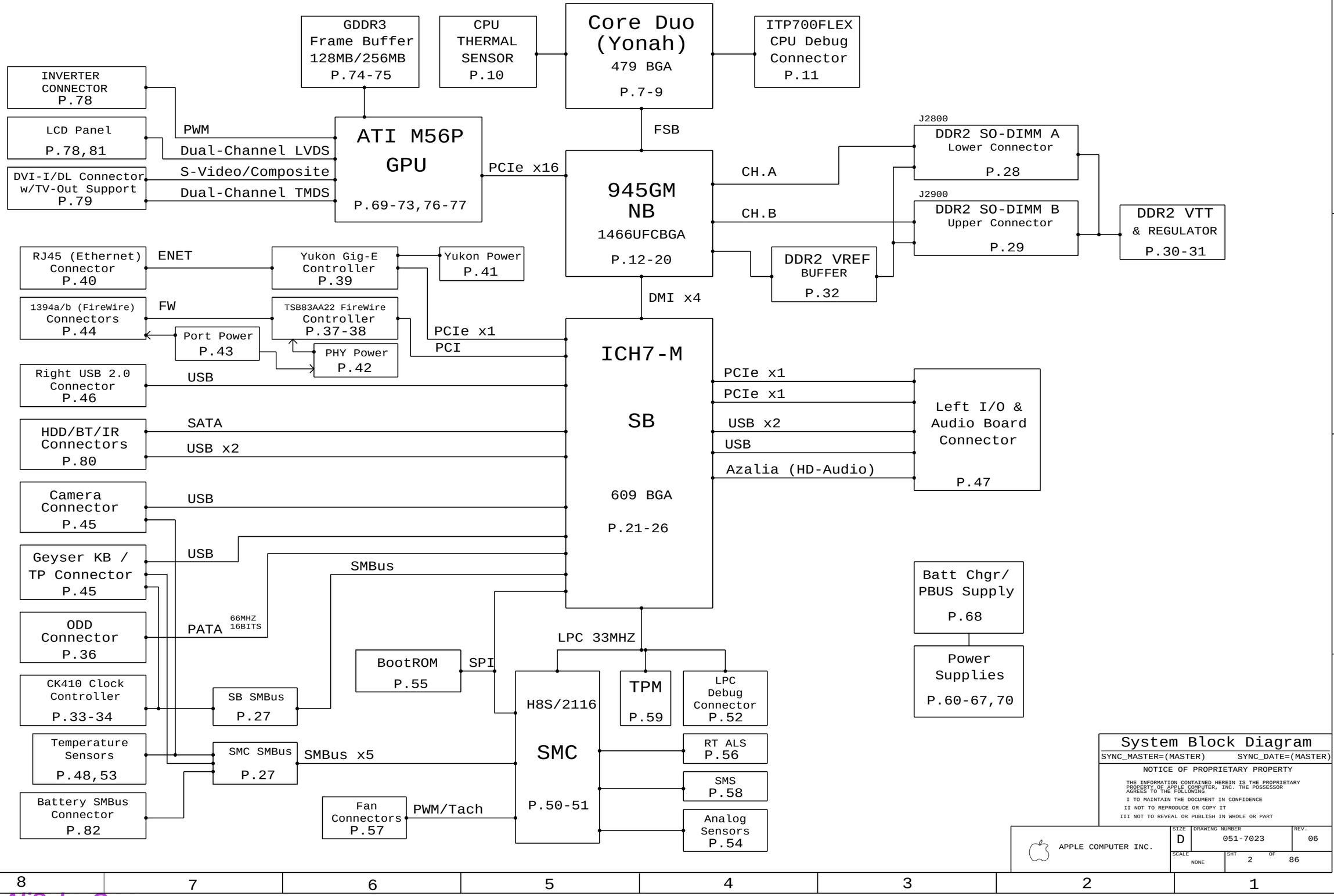

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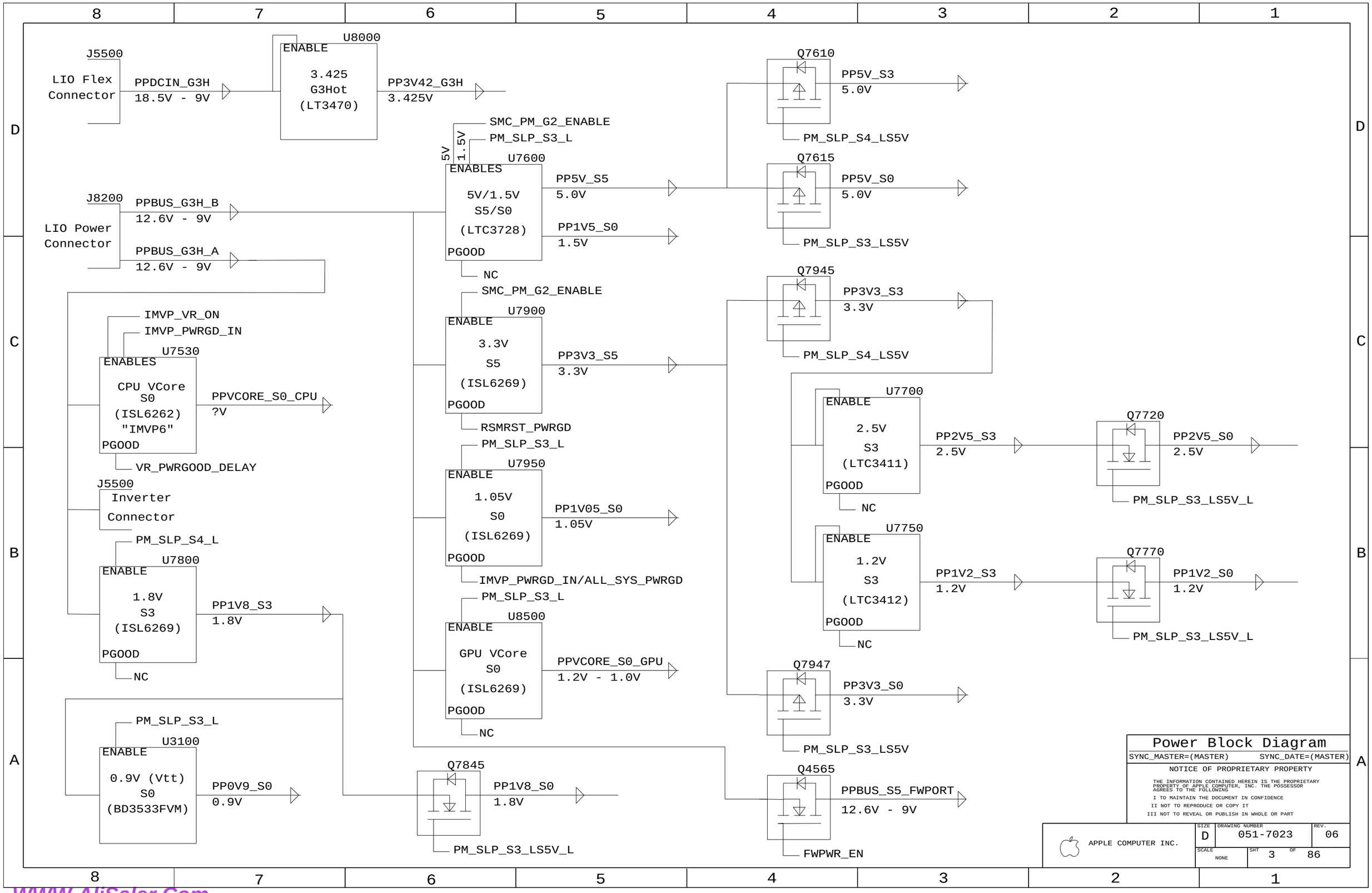

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BOM NUMBER	BOM NAME	BOM OPTIONS
630-7404	PCBA,SULLY,2.0GHz,M9	VRAM_256SAM,M9_COMMON,CPU_2_0GHZ,EEE_UNZ
630-7406	PCBA,SULLY,2.16GHz,M9	VRAM_256SAM,M9_COMMON,CPU_2_16GHZ,EEE_UP1

BOM GROUP	BOM OPTIONS
VRAM_128SAM	VRAM_128_SAMSUNG
VRAM_256SAM	GPU_MEM_256M,VRAM_256_SAMSUNG
VRAM_128HY	GPU_MEM_HYNIX,VRAM_128_HYNIX
VRAM_256HY	GPU_MEM_HYNIX,GPU_MEM_256M,VRAM_256_HYNIX

BOM GROUP	BOM OPTIONS
M9_COMMON	ALTERNATE,COMMON,M9_COMMON1,M9_COMMON2,M9_COMMON3,M9_COMMON4,M9_DEBUG
M9_COMMON1	ENET_LOM_DISABLE,ENETPWR_S3AC,GPUTHM_A_GPU,GPU_BB_CTL,HSTHMSNS_HAS,INVERTER_BUF,ONEWIRE_PU
M9_COMMON2	KBDLED_HAS,MEMVREF_S3,MEMVTT_EN_PU,RTUSB_ESD,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
M9_COMMON3	LVDS_PD,M56_REV_B24_LP,FW_B_BILINGUAL,FW_A_DS_ONLY,FW_PORT_FAULT_PU,FW_PLTRST_UNGATED
M9_COMMON4	LIO_TEMP,BOOTROM_DEVEL,SMC_DEVEL
M9_DEBUG	ITP,ITPCONN,LPCPLUS

Bar Code Labels / EEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UNZ]	CRITICAL	EEE_UNZ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UP0]	CRITICAL	EEE_UP0
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UP1]	CRITICAL	EEE_UP1
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UP2]	CRITICAL	EEE_UP2
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:UYU]	CRITICAL	EEE_UYU

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0266	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	M56_REV_B24_LL
338S0302	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	M56_REV_B24_HL
338S0309	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	M56_REV_B24_LP
338S0315	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	M56_REV_B26_LP
338S0316	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	M56_REV_B26_P
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX

PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0309	338S0266	M56_REV_B24_LL	U8400	LP is alt to LL
338S0266	338S0309	M56_REV_B24_LP	U8400	LL is alt to LP
338S0315	338S0309	M56_REV_B24_LP	U8400	B26_LP is alt to B24_LP
376S0448	376S0445		ALL	Vishay 2nd source
128S0083	128S0073		C2516	1.86 max alt to 1.9 max
128S0093	128S0092		ALL	Kemet is alt to Sanyo
128S0060	128S0094		ALL	Sanyo is alt to Panasonic
128S0095	128S0094		ALL	330uF,2V,6MOHM,D2
128S0081	128S0061		ALL	C2 package is alt to C3

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1876	1	IC,SMC,PRGRM,M9	U5800	CRITICAL	SMC_DEVEL
341S1876	1	IC,SMC,PRGRM,M9	U5800	CRITICAL	SMC_FINAL
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
335S0384	1	IC,16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	CRITICAL	BOOTROM_BLANK
341S1828	1	IC,EFI,BOOTROM DEVELOPMENT,M9	U6301	CRITICAL	BOOTROM_DEVEL
341S1829	1	IC,EFI,BOOTROM FINAL,M9	U6301	CRITICAL	BOOTROM_FINAL
353S1235	1	IC,CPU VOLTAGE REGULATOR,IMVP,TWO PHASE	U7530	CRITICAL	
359S0101	1	IC,CY28445-5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3282	1	IC,CPU,479 BGA	U0700	CRITICAL	CPU_1_83GHZ
337S3267	1	IC,CPU,479 BGA	U0700	CRITICAL	CPU_2_0GHZ
337S3268	1	IC,CPU,479 BGA	U0700	CRITICAL	CPU_2_16GHZ
338S0269	1	IC,945GM,SOUTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	

M9 Specific Aliases

PPBUS_G3H — PPBUS_G3H
PPDCIN_G3H — PPDCIN_G3H
PPDCIN_G3H
SMC_RSTGATE_L (MAKE_BASE=TRUE) — SMC_RSTGATE_L
PPFW_PORTA_VP_UF (MAKE_BASE=TRUE) — PPFW_PORTA_VP_UF
PPFW_PORTB_VP_UF (MAKE_BASE=TRUE) — PPFW_PORTB_VP_UF
PP3V3_S0 — PP3V3_S0
PP3V3_S0
PP3V3_S0
SMBUS_SMC_B_S0_SCL — SMBUS_SMC_B_S0_SCL
SMBUS_SMC_B_S0_SDA — SMBUS_SMC_B_S0_SDA
PCI_AD<19> (MAKE_BASE=TRUE) — =FW_PCI_IDSEL
PP5V_S0 — PP5V_S0
PPBUS_S5_FW_FET — PPBUS_S5_FW_FET
PPBUS_S5_FW_FET
PPBUS_S5_FW_FET
PP3V3_FWPHY — PP3V3_FWPHY (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, MAKE_BASE=TRUE)
PP3V3_FWPHY
PP3V3_FWPHY
PP3V3_FWPHY
PP3V3_FWPHY
PP1V95_FWPHY — PP1V95_FWPHY (VOLTAGE=1.95V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, MAKE_BASE=TRUE)
PP1V95_FWPHY
PP1V8_S3 — PP1V8_S3
LT2USB_OC_L (MAKE_BASE=TRUE) — LT2USB_OC_L
PCI_GNT3_L (MAKE_BASE=TRUE) — PCI_GNT3_L
PCI_REQ3_L (MAKE_BASE=TRUE) — PCI_REQ3_L

BOM Configuration

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7023	06
SCALE: NONE	SHT 4 OF 86	

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Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	60
TRUE		P5VS5_RUNSS	61 65
TRUE		P1V5S0_RUNSS	61 65
TRUE		P2V5S3_MODE	62
TRUE		P2V5S3_SHDNRT	62
TRUE		P1V2S3_RT	62
TRUE		P1V2S3_RUNSS	41 62
TRUE		P1V8S3_COMP	63
TRUE		P1V8S3_FSET	63
TRUE		P3V3S5_COMP	64
TRUE		P3V3S5_FSET	64
TRUE		P1V05S0_COMP	64
TRUE		P1V05S0_FSET	64
TRUE		P3V42G3H_FB	65
TRUE		GPUVCORE_COMP	70
TRUE		GPUVCORE_FSET	70
TRUE		GPUBBP_ADJ	70

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7 12 86
TRUE		FSB_ADS_L	7 12 86
TRUE	TRUE	FSB_ADSTB_L<1..0>	7 12 86
TRUE		FSB_BNR_L	7 12 86
TRUE		FSB_BREQ0_L	7 12 86
TRUE		FSB_D_L<63..0>	7 12 86
TRUE		FSB_DBSY_L	7 12 86
TRUE	TRUE	FSB_DINV_L<3..0>	7 12 86
TRUE		FSB_DRDY_L	7 12 86
TRUE	TRUE	FSB_DSTBN_L<3..0>	7 12 86
TRUE	TRUE	FSB_DSTBP_L<3..0>	7 12 86
TRUE		FSB_HIT_L	7 12 86
TRUE		FSB_HITM_L	7 12 86
TRUE		FSB_LOCK_L	7 12 86
TRUE		FSB_REQ_L<4..0>	7 12 86

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14 22
TRUE	DMI_N2S_N<1..0>	14 22
TRUE	SB_CLK100M_SATA_P	21 34
TRUE	SB_CLK100M_SATA_N	21 34

Power Nets

FUNC_TEST		
TRUE	PP0V9_S0	30 31 65 66
TRUE	PP1V05_S0	5 7 8 9 11 12 13 16 17 19 21 24 29 34 54 64 66
TRUE	PP1V2_S0	62 65 66 69 76
TRUE	PP1V2_S3	5 39 62 66
TRUE	PP1V5_S0	5 8 9 13 16 17 19 24 25 47 65 66
TRUE	PP1V8_S0	63 65 66
TRUE	PP1V8_S3	4 5 14 16 19 28 29 31 32 37 54 63 66
TRUE	PP2V5_S0	17 19 62 65 66 76 77
TRUE	PP2V5_S3	39 62 66
TRUE	PP3V3_S0	78 79 80 41 51 53 56 57 59 60 64 65 66
TRUE	PP3V3_S3	4 5 10 14 17 19 20 21 22 23 24 25 26 27 28 29 33 34 36 37 43
TRUE	PP3V3_S5	27 32 37 41 45 51 56 58 59 62 63 64 66 80
TRUE	PP5V_S0	11 22 23 24 25 26 55 62 64 65 66 78 79 80
TRUE	PP5V_S3	4 5 29 31 36 37 47 52 54 56 57 60 61 65 66 67 78
TRUE	PP5V_S5	5 45 51 61 66 80
TRUE	PPBUS_G3H	5 25 46 51 61 63 64 65 66 67 70
TRUE	GND	4 5 21 43 47 54 60 61 63 64 65 66 70 78

Request for at least 10 GND TPs

Characterization TPs

FUNC_TEST		
TRUE	IMVP_VR_ON	50 60
TRUE	IMVP_DPRSLPVR	60 86
TRUE	PM_SLP_S3_L	23 32 39 43 50 54 64 65
TRUE	PM_SLP_S3BATT	41
TRUE	PM_SLP_S4_L	5 23 41 46 47 50 63 65
TRUE	PM_SLP_S5_L	23 50 51
TRUE	P1V5P1V05S0_PGOOD	60 64 65
TRUE	CPU_DPRSTP_L	7 21 60
TRUE	IMVP6_VID<6..0>	9 60
TRUE	FSB_CLK_CPU_N	7 34
TRUE	FSB_CLK_CPU_P	7 34
TRUE	PLT_RST_L	5 14 22 26
TRUE	PLT_RST_L	5 14 22 26
TRUE	PEG_RESET_L	26 69
TRUE	SMC_LRESET_L	26 50
TRUE	TPM_LRESET_L	26 59
TRUE	CPU_STPCLK_L	7 21 86
TRUE	FSB_CLK_NB_P	12 34
TRUE	FSB_CLK_NB_N	12 34
TRUE	CLK_NB_OE_L	14 33
TRUE	NB_CLK100M_GCLKIN_P	14 34
TRUE	NB_CLK100M_GCLKIN_N	14 34
TRUE	GND	
TRUE	GND	
TRUE	GND	
TRUE	GND	
TRUE	CPU_THERMTRIP_R	21
TRUE	TP_SB_SUS_CLK	6 23

MAC-1 TPs

FUNC_TEST		
TRUE	CPU_PWRGD	7 21 86
TRUE	TP_CPU_CPUSLP_L	21
TRUE	PM_DPRSLPVR	14 23 60 86
TRUE	CPU_DPSLP_L	7 21 86
TRUE	PM_LAN_ENABLE	23 50
TRUE	PCI_RST_L	22 37
TRUE	PM_RSMRST_L	23 50
TRUE	PM_SB_PWROK	23 26
TRUE	SB_RTC_RST_L	21 26
TRUE	PM_STPCPU_L	23 33
TRUE	PM_STPPCI_L	23 33
TRUE	VR_PWRGD_CK410	23 26
TRUE	VR_PWRGOOD_DELAY	14 26 60
TRUE	FSB_CPURST_L	7 11 12 86
TRUE	FSB_SLPCPU_L	7 12
TRUE	FSB_DPWR_L	7 12 86
TRUE	NB_SB_SYNC_L	14 22
TRUE	PP2V5_S0_GPU_TPVDD	77
TRUE	PP2V5_S0_GPU_TXVDDR	77
TRUE	PP2V5_S0_GPU_AVDD	77
TRUE	PP2V5_S0_GPU_A2VDD	77
TRUE	PP2V5_S0_GPU_LPVDD	77
TRUE	PP2V5_S0_GPU_LVDDR	59 60 64 65 66 70 78 79
TRUE	PP3V3_S0	23 32 39 43 50 54 64 65 4 5 10 14 17 19 20 21 22 23 24 25 26 27 28 29 33 34 36 37 43 48 51 53 56 57 (=PP3V3_S0_CK410)
TRUE	PP3V3_S0_CK410_VDD48	33
TRUE	PP3V3_S0_CK410_VDD_PCI	33
TRUE	PP3V3_S0_CK410_VDD_REF	33
TRUE	PP3V3_S0_CK410_VDD_CPU_SRC	33
TRUE	PP3V3_S0_CK410_VDDA	33
TRUE	PP3V3_FWPHY	4 38 42 43 44
TRUE	PP3V3_FWPHY_AVDD	38
TRUE	PP3V3_FWPHY_PLLVDD	38
TRUE	PP1V95_FWPHY	4 38 42
TRUE	PP1V95_FWPHY_PLLVDD	38
TRUE	PP1V2_S3	5 39 62 66 (=PP1V2_S3_ENET)
TRUE	PP3V3_S3AC	39 41 66 (=PP3V3_S3_ENET)
TRUE	PP2V5_S3	5 39 62 66 (=PP2V5_S3_ENET)
TRUE	PP2V5_S3_ENET_AVDD	39 40

Fan Connectors

FUNC_TEST		
TRUE	PP5V_S0	66 67 70 78 79 80 4 5 29 31 36 37 47 52 54 56 57 60 61 65
TRUE	FAN_LT_PWM	57
TRUE	FAN_LT_TACH	57
TRUE	FAN_RT_PWM	57
TRUE	FAN_RT_TACH	57

LPC+ Debug Connector

FUNC_TEST		
TRUE	PP3V42_G3H	68 5 26 27 35 45 50 51 52 54 65 66
TRUE	PP5V_S0	66 67 70 78 79 80 4 5 29 31 36 37 47 52 54 56 57 60 61 65
TRUE	LPC_AD<0>	21 50 52 59
TRUE	LPC_AD<1>	21 50 52 59
TRUE	LPC_FRAME_L	21 50 52 59
TRUE	PM_CLKRUN_L	23 50 52 59
TRUE	BOOT_LPC_SPI_L	22 50 52
TRUE	SMC_TMS	50 51 52
TRUE	DEBUG_RST_L	26 52
TRUE	SMC_TRST_L	50 52
TRUE	SMC_TDO	50 51 52
TRUE	SMC_MD1	50 52
TRUE	SMC_TX_L	50 51 52
TRUE	FWH_INIT_L	21 50 51 52
TRUE	PCI_CLK_PORT80_LPC	34 52
TRUE	LPC_AD<2>	21 50 52 59
TRUE	LPC_AD<3>	21 50 52 59
TRUE	INT_SERIRQ	23 50 52 59
TRUE	PM_SUS_STAT_L	23 50 51 52 59
TRUE	SMC_TDI	50 51 52
TRUE	SMC_TCK	50 51 52
TRUE	SMC_RST_L	50 51 52
TRUE	SMC_NMI	50 52
TRUE	SMC_RX_L	50 51 52
TRUE	SV_SET_UP	23 52

Resistor Calibration

FUNC_TEST		
TRUE	PP5V_S0	66 67 70 78 79 80 4 5 29 31 36 37 47 52 54 56 57 60 61 65
TRUE	PP1V8_S3	64 66
TRUE	PP1V05_S0	5 7 8 9 11 12 13 16 17 19 21 24 29 34 54
TRUE	PPVCORE_S0_CPU	8 9 54 60 66
TRUE	PPVCORE_S0_GPU	54 66 70 71 76
TRUE	ISENSE_CAL_EN	50 54
TRUE	GND	

Request for at least 2 GND TPs per resistor

Camera Connector

FUNC_TEST		
TRUE	PP5V_S3	5 45 51 61 66 80
TRUE	USB2_CAMERA_N	6 22 45
TRUE	USB2_CAMERA_P	6 22 45
TRUE	SMBUS_SMC_0_S0_SDA	27 45 50 53
TRUE	SMBUS_SMC_0_S0_SCL	27 50 53

Thermal Sensors

FUNC_TEST		
TRUE	HSTHMSNS_DX_P	53
TRUE	HSTHMSNS_DX_N	53
TRUE	RSFSTHMSNS_D_P	53
TRUE	RSFSTHMSNS_D_N	53

SMC TPs

FUNC_TEST		
TRUE	PM_SYSRST_L	23 26 50
TRUE	SMC_ONOFF_L	45 50 51 54

Battery Connector

FUNC_TEST		
TRUE	BATT_POS	67 68
TRUE	BATT_NEG	67 68
TRUE	SMC_BS_ALRT_L	50 51 67
TRUE	SMBUS_SMC_BSA_SCL	27 50 67
TRUE	SMBUS_SMC_BSA_SDA	27 50 67

Left I/O Data Connector

FUNC_TEST		
TRUE	PP1V5_S0	25 47 65 66 5 8 9 13 16 17 66 67 70 78 79 80
TRUE	PPBUS_G3H	68 70 78 79 80
TRUE	PP3V42_G3H	4 5 41 43 47 54 60 61 63 64 66
TRUE	PP5V_S0_AUDIO	5 26 27 35 45 50 51 54 65 66
TRUE	GND_AUDIO	47
TRUE	ALS_GAIN	6 47 50
TRUE	LTALS_OUT	47 56
TRUE	ACZ_SDATAIN<0>	21 47 86
TRUE	ACZ_SDATAOUT	21 47 86
TRUE	ACZ_BITCLK	21 47 86
TRUE	ACZ_RST_L	21 47 86
TRUE	EXCARD_OC_L	6 22 47 51
TRUE	LTUSB_OC_L	6 22 47
TRUE	LT2USB_OC_L	4 22 47
TRUE	PM_SLP_S3_LS5V	47 61 65
TRUE	PM_SLP_S4_L	5 23 41 46 47 50 63 65
TRUE	SYS_ONEWIRE	47 50 51
TRUE	MINI_CLKREQ_L	33 34 47
TRUE	SMC_EXCARD_CP	47 50 51
TRUE	EXCARD_CLKREQ_L	33 34 47
TRUE	SMC_EXCARD_PWR_EN	47 50
TRUE	LIO_PLT_RESET_L	26 47
TRUE	ACZ_SYNC	21 47 86
TRUE	USB2_LT_N	6 22 47
TRUE	USB2_LT_P	6 22 47
TRUE	USB2_LT2_N	6 22 47
TRUE	USB2_LT2_P	6 22 47
TRUE	PCIE_MINI_R2D_C_N	47 49
TRUE	PCIE_MINI_R2D_C_P	47 49
TRUE	PCIE_MINI_D2R_N	22 47 49
TRUE	PCIE_MINI_D2R_P	22 47 49
TRUE	PCIE_CLK100M_MINI_P	34 47
TRUE	PCIE_CLK100M_MINI_N	34 47
TRUE	SMBUS_SB_SCL	23 27 28 29 33 45 47
TRUE	SMBUS_SB_SDA	23 27 28 29 33 45 47
TRUE	PCIE_WAKE_L	23 39 47
TRUE	SMC_BC_ACOK	47 50 51 67 68

Left I/O Power Connector

FUNC_TEST		
TRUE	PP18V5_DCIN	67
TRUE	PP5V_S5	5 25 46 51 61 63 64 65 66 67 70
TRUE	PP5V_S0_AUDIO_PWR	67
TRUE	GND_AUDIO_PWR	67
TRUE	GND	

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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NC_CPU_A32_L — NC_CPU_A32_L
NC_CPU_A33_L — NC_CPU_A33_L
NC_CPU_A34_L — NC_CPU_A34_L
NC_CPU_A35_L — NC_CPU_A35_L
NC_CPU_A36_L — NC_CPU_A36_L
NC_CPU_A37_L — NC_CPU_A37_L
NC_CPU_A38_L — NC_CPU_A38_L
NC_CPU_A39_L — NC_CPU_A39_L
NC_CPU_APM0_L — NC_CPU_APM0_L
NC_CPU_APM1_L — NC_CPU_APM1_L
NC_CPU_EXTBREF — NC_CPU_EXTBREF
NC_CPU_HFPLL — NC_CPU_HFPLL
NC_CPU_SPARE0 — NC_CPU_SPARE0
NC_CPU_SPARE1 — NC_CPU_SPARE1
NC_CPU_SPARE2 — NC_CPU_SPARE2
NC_CPU_SPARE4 — NC_CPU_SPARE4

MAKE_BASE=TRUE
NO_TEST=TRUE

NC_MEM_A_A<15..14> — MEM_A_A<15..14>
NC_MEM_B_A<15..14> — MEM_B_A<15..14>

TP_NB_CFG<4..3> — NB_CFG<4..3>
TP_NB_CFG<6> — NB_CFG<6>
TP_NB_CFG<8> — NB_CFG<8>
TP_NB_CFG<11..10> — NB_CFG<11..10>
TP_NB_CFG<15..14> — NB_CFG<15..14>
TP_NB_CFG<17> — NB_CFG<17>

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> — NB_CFG<13..12>

TP_SB_SUS_CLK — TP_SB_SUS_CLK

R0600
0
5%
1/16W
MF-LF
402

ALS_GAIN — RTALS_GAIN — RTALS_GAIN

NC_ENET_CTRL12 — NC_ENET_CTRL12
NC_ENET_CTRL25 — NC_ENET_CTRL25

Ethernet Powr Management Support

ENET_LOM_DISABLE
R0690
0
5%
1/16W
MF-LF
402

SB_GPIO30 — ENET_LOM_DIS_L

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOM_DISABLE" are mutually-exclusive.

USB Port "A" (Debug Port) = Right USB 2.0 Port

USB2_RT_P — USB2_RT_P — USB2_RT_P
USB2_RT_N — USB2_RT_N — USB2_RT_N
RTUSB_OC_L — RTUSB_OC_L — RTUSB_OC_L

USB Port "B" = Trackpad (Geyser)

USB_TRACKPAD_P — USB_TRACKPAD_P — USB_TRACKPAD_P
USB_TRACKPAD_N — USB_TRACKPAD_N — USB_TRACKPAD_N
UNUSED_USB_B_OC_L — UNUSED_USB_B_OC_L

USB Port "C" = Left USB 2.0 Port

USB2_LT_P — USB2_LT_P — USB2_LT_P
USB2_LT_N — USB2_LT_N — USB2_LT_N
LTUSB_OC_L — LTUSB_OC_L

USB Port "D" = Camera

USB2_CAMERA_P — USB2_CAMERA_P — USB2_CAMERA_P
USB2_CAMERA_N — USB2_CAMERA_N — USB2_CAMERA_N
UNUSED_USB_D_OC_L — UNUSED_USB_D_OC_L

USB Port "E" = ExpressCard

USB2_EXCARD_P — USB2_EXCARD_P — USB2_EXCARD_P
USB2_EXCARD_N — USB2_EXCARD_N — USB2_EXCARD_N
EXCARD_OC_L — EXCARD_OC_L

USB Port "F" = IR Receiver

USB_IR_P — USB_IR_P — USB_IR_P
USB_IR_N — USB_IR_N — USB_IR_N

USB Port "G" = Bluetooth (M13P)

USB_BT_P — USB_BT_P — USB_BT_P
USB_BT_N — USB_BT_N — USB_BT_N

USB Port "H" = 2nd Left USB 2.0 Port

USB2_LT2_P — USB2_LT2_P — USB2_LT2_P
USB2_LT2_N — USB2_LT2_N — USB2_LT2_N

MAKE_BASE=TRUE

Chassis connection to be made at the fan cutout near the right ALS

SH0601
EMI-SPRING
0G-502620R

GND_CHASSIS_FANFRAME
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

R0601
0
5%
1/16W
MF-LF
402

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25

GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_DVI_TOP
GND_CHASSIS_DVI_TOP
GND

Chassis connection to be made on FW shell

ZT0603
HOLE-VIA-P5RP25

GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_DVI_BOT
GND_CHASSIS_DVI_BOT
GND_CHASSIS_DVI_BOT
GND_CHASSIS_DVI_BOT

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25

GND_CHASSIS_USB
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_USB
GND_CHASSIS_USB
GND_CHASSIS_USB

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25

GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_LVDS
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS

SH0600
OG-503040
SHLD-SM-LF

GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE

GND_CHASSIS_INVERTER

Signal Aliases

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/11/2005)

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OMIT

U0700
YONAH
CPU
BGA
(1 OF 4)

ADDR GROUP0
CONTROL
ADDR GROUP1
XDP/ITP SIGNALS
THERM
HCLK
RESERVED

FSB_A_L<3> J4 A3*
FSB_A_L<4> L4 A4*
FSB_A_L<5> M3 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M1 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L1 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> U2 ADSTB0*

FSB_REQ_L<0> K3 REQ0*
FSB_REQ_L<1> H2 REQ1*
FSB_REQ_L<2> K2 REQ2*
FSB_REQ_L<3> J3 REQ3*
FSB_REQ_L<4> L5 REQ4*

FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U2 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W3 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> W2 A30*
FSB_A_L<31> Y1 A31*
FSB_ADSTB_L<1> AA2 ADSTB1*

CPU_A20M_L A6 A20M*
CPU_FERR_L A5 FERR*
CPU_IGNNE_L C4 IGNNE*
CPU_STPCLK_L D5 STPCLK*
CPU_INTR C6 LINT0
CPU_NMI B4 LINT1
CPU_SMI_L A3 SMI*

NC_CPU_A32 AA1 RSVD1
NC_CPU_A33 AA4 RSVD2
NC_CPU_A34 AB2 RSVD3
NC_CPU_A35 AA3 RSVD4
NC_CPU_A36 M4 RSVD5
NC_CPU_A37 N5 RSVD6
NC_CPU_A38 T2 RSVD7
NC_CPU_A39 V3 RSVD8
NC_CPU_APM0 B2 RSVD9
NC_CPU_APM1 C3 RSVD10
NC_CPU_HFPLL B25 RSVD11

ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 FSB_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* B1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC A25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

RSVD12 T22 NC_CPU_EXTBREF
RSVD13 D2 NC_CPU_SPARE0
RSVD14 F6 NC_CPU_SPARE1
RSVD15 D3 NC_CPU_SPARE2
RSVD16 C1 TP_CPU_SPARE3
RSVD17 AF1 NC_CPU_SPARE4
RSVD18 D22 TP_CPU_SPARE5
RSVD19 C23 TP_CPU_SPARE6
RSVD20 C24 TP_CPU_SPARE7

SPARE[7-0],HFPLL:
ROUTE TO TP VIA AND
PLACE GND VIA W/IN 1000 MILS

PP1V05_S0

R0702 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON
FSB_IERR_L WITH A GND
0.1" AWAY

R0703 54.9 1% 1/16W MF-LF 402

R0704 68 5% 1/16W MF-LF 402
CPU_PROCHOT_L TO SMC
AND CPU VR TO INFORM
CPU IS HOT

PM_THRMTRIP#
SHOULD CONNECT TO
ICH7-M AND GMCH
WITHOUT T-ING (NO
STUB)

R0705 1K 1% 1/16W MF-LF 402
CPU_GTLREF

R0706 2.0K 1% 1/16W MF-LF 402
LAYOUT NOTE: 0.5" MAX LENGTH
CPU_TEST1
CPU_TEST2
CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>

R0720 54.9 1% 1/16W MF-LF 402 XDP_TMS
R0721 54.9 1% 1/16W MF-LF 402 XDP_TDI
R0722 54.9 1% 1/16W MF-LF 402 XDP_TCK

NOSTUFF R0730 0 402
R0712 5K 5% 1/16W MF-LF 402
NOSTUFF R0707 1K 5% 1/16W MF-LF 402

OMIT

U0700
YONAH
CPU
BGA
(2 OF 4)

DATA GRP0
DATA GRP2
DATA GRP1
DATA GRP3
MISC

FSB_D_L<0> E22 D0*
FSB_D_L<1> F24 D1*
FSB_D_L<2> E26 D2*
FSB_D_L<3> H22 D3*
FSB_D_L<4> F23 D4*
FSB_D_L<5> G25 D5*
FSB_D_L<6> E25 D6*
FSB_D_L<7> E23 D7*
FSB_D_L<8> K24 D8*
FSB_D_L<9> G24 D9*
FSB_D_L<10> J24 D10*
FSB_D_L<11> J23 D11*
FSB_D_L<12> H26 D12*
FSB_D_L<13> F26 D13*
FSB_D_L<14> K22 D14*
FSB_D_L<15> H25 D15*
FSB_DSTBN_L<0> L23 DSTBN0*
FSB_DSTBP_L<0> L22 DSTBP0*
FSB_DINV_L<0> G26 DINV0*

FSB_D_L<16> N22 D16*
FSB_D_L<17> K25 D17*
FSB_D_L<18> P26 D18*
FSB_D_L<19> R23 D19*
FSB_D_L<20> L25 D20*
FSB_D_L<21> L22 D21*
FSB_D_L<22> L23 D22*
FSB_D_L<23> M23 D23*
FSB_D_L<24> P25 D24*
FSB_D_L<25> P22 D25*
FSB_D_L<26> P23 D26*
FSB_D_L<27> T24 D27*
FSB_D_L<28> R24 D28*
FSB_D_L<29> L26 D29*
FSB_D_L<30> T25 D30*
FSB_D_L<31> N24 D31*
FSB_DSTBN_L<1> M24 DSTBN1*
FSB_DSTBP_L<1> N25 DSTBP1*
FSB_DINV_L<1> U26 DINV1*

AD26 GTLREF
A2 NC
C26 TEST1
D25 TEST2
B22 BSEL0
B23 BSEL1
C21 BSEL2

D32* AA23 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* W25 FSB_D_L<36>
D37* U23 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U22 FSB_D_L<39>
D40* AB25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* AA26 FSB_D_L<43>
D44* Y26 FSB_D_L<44>
D45* Y22 FSB_D_L<45>
D46* AC26 FSB_D_L<46>
D47* AA24 FSB_D_L<47>
DSTBN2* W24 FSB_DSTBN_L<2>
DSTBP2* Y25 FSB_DSTBP_L<2>
DINV2* V23 FSB_DINV_L<2>

D48* AC22 FSB_D_L<48>
D49* AC23 FSB_D_L<49>
D50* AB22 FSB_D_L<50>
D51* AA21 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC25 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AD24 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AE25 FSB_D_L<60>
D61* AF25 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AF26 FSB_D_L<63>
DSTBN3* AD23 FSB_DSTBN_L<3>
DSTBP3* AE24 FSB_DSTBP_L<3>
DINV3* AC20 FSB_DINV_L<3>

COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 U1 CPU_COMP<2>
COMP3 V1 CPU_COMP<3>

DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_SLPCPU_L
PSI* AE6 CPU_PSI_L

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE
TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE
TRACE LENGTH SHORTER THAN 0.5".

R0716 27.4 1% 1/16W MF-LF 402
R0717 54.9 1% 1/16W MF-LF 402
R0718 27.4 1% 1/16W MF-LF 402
R0719 54.9 1% 1/16W MF-LF 402

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

CPU 1 OF 2-FSB

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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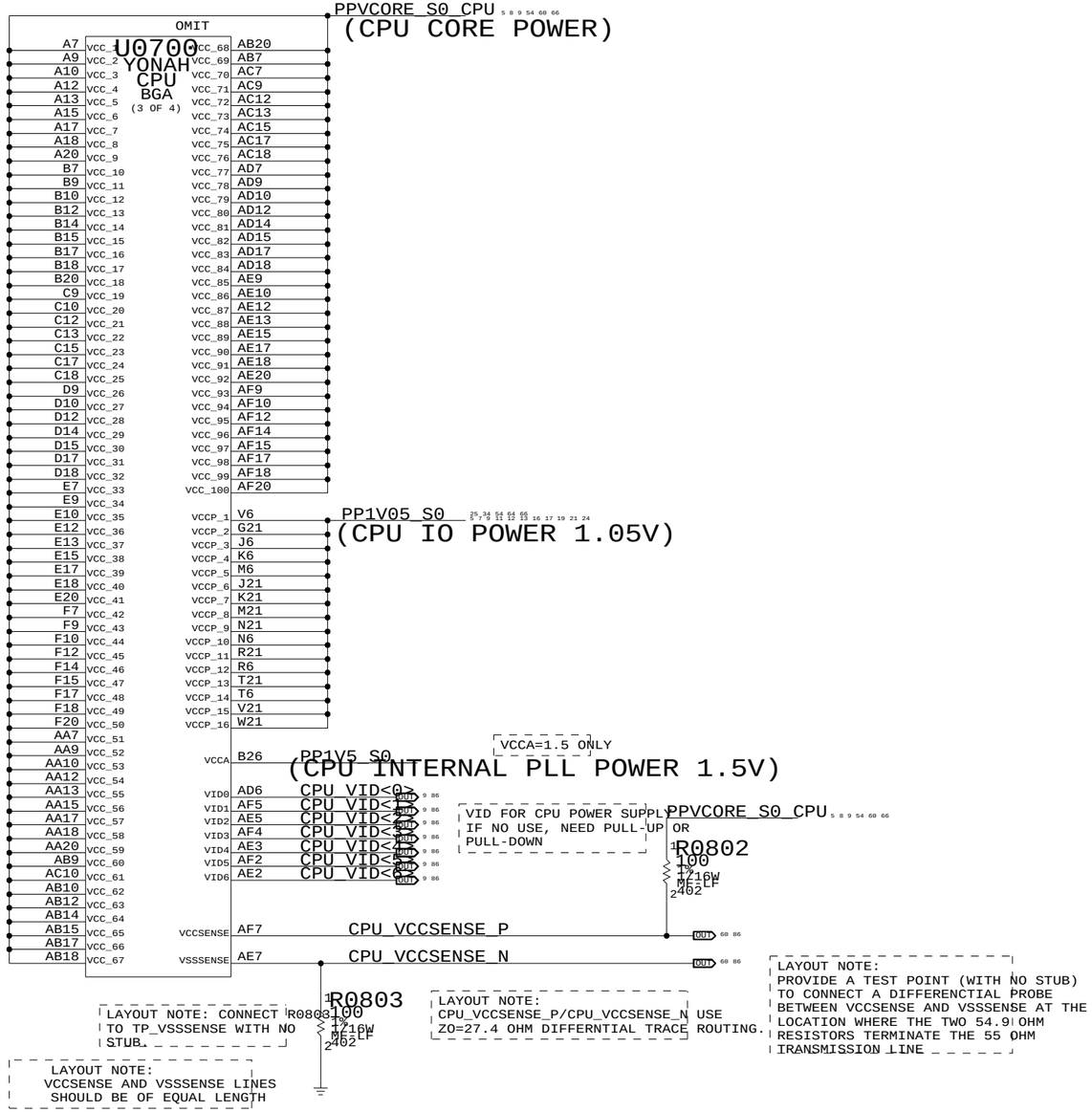

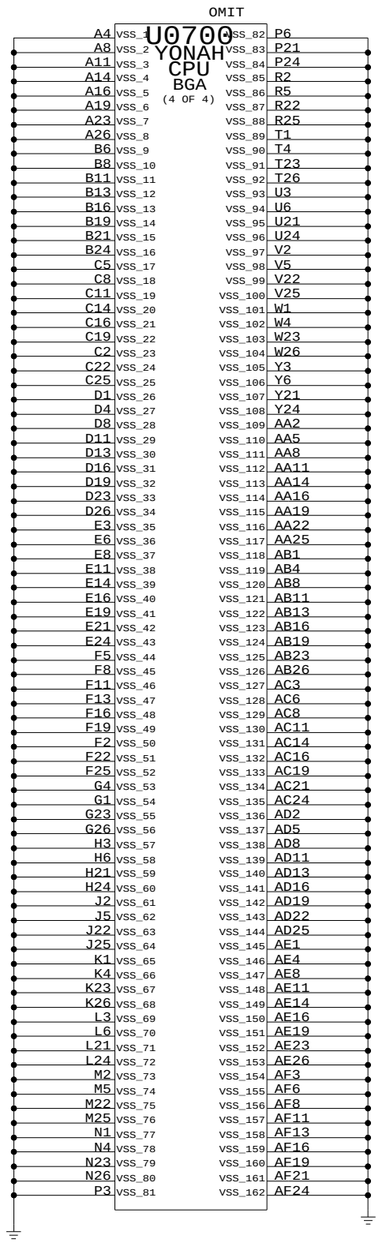

CPU 2 OF 2-PWR/GND

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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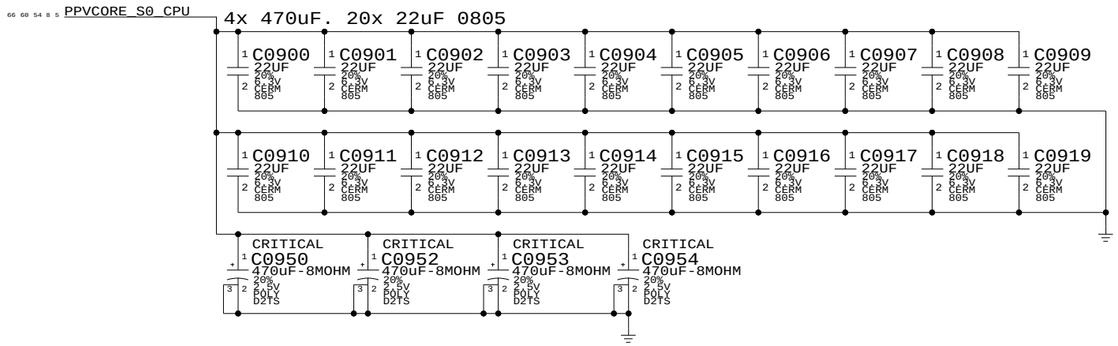
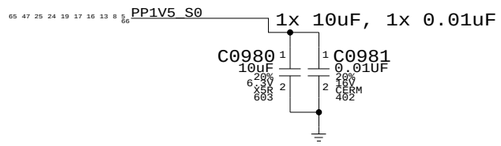
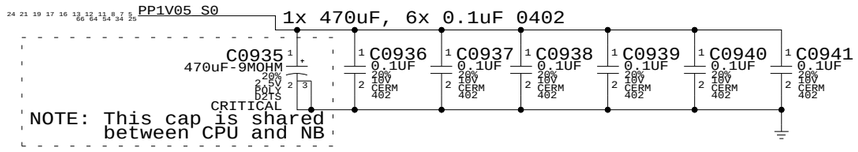
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

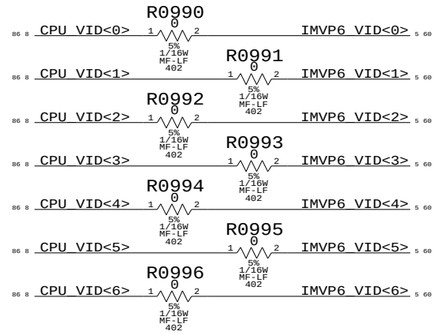


VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production


R0990 0 5% 1/16W MF-LF 402
CPU VID<0> IMVP6 VID<0>
R0991 0 5% 1/16W MF-LF 402
CPU VID<1> IMVP6 VID<1>
R0992 0 5% 1/16W MF-LF 402
CPU VID<2> IMVP6 VID<2>
R0993 0 5% 1/16W MF-LF 402
CPU VID<3> IMVP6 VID<3>
R0994 0 5% 1/16W MF-LF 402
CPU VID<4> IMVP6 VID<4>
R0995 0 5% 1/16W MF-LF 402
CPU VID<5> IMVP6 VID<5>
R0996 0 5% 1/16W MF-LF 402
CPU VID<6> IMVP6 VID<6>
86 8 5 60

CPU Decoupling & VID

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CPU ZONE THERMAL SENSOR

LAYOUT NOTE:
ADD GND GUARD TRACE
FOR CPU_THERMD_P AND
CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND
CPU_THERMD_N ON SAME
LAYER.
10 MIL TRACE
10 MIL SPACING

PLACEHOLDER ADT7461A

PP3V3_S0

C1002
0.1UF
16V
10%
X5R
402

R1005
10K
5%
1/16W
MF-LF
402

R1006
10K
5%
1/16W
MF-LF
402

CRITICAL

U1001
ADT7461
MSOP

VDD
GND
ALERT*/THM2*
THM*
SCLK
SDATA
D+
D-

THRM_ALERT_L
THRM_ALERT

SMBUS_SMC_B_S0_SCL
SMBUS_SMC_B_S0_SDA

(TO CPU INTERNAL THERMAL DIODE)

CPU_THERMD_P
CPU_THERMD_N

R1001
499
1%
1/16W
MF-LF
402

R1002
499
1%
1/16W
MF-LF
402

C1001
0.001UF
16V
10%
CERM
402

THRM_CPU_DX_P
THRM_CPU_DX_N

PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

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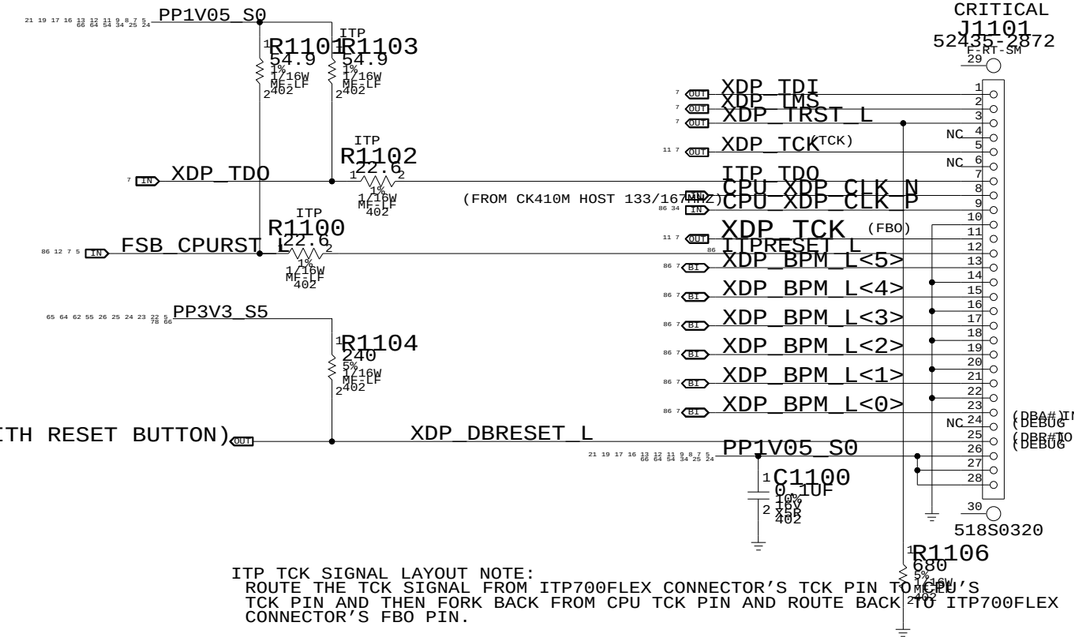
CPU ITP700FLEX DEBUG SUPPORT



ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=MSYNC SYNC_DATE=02/10/2006

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NONE	11	86

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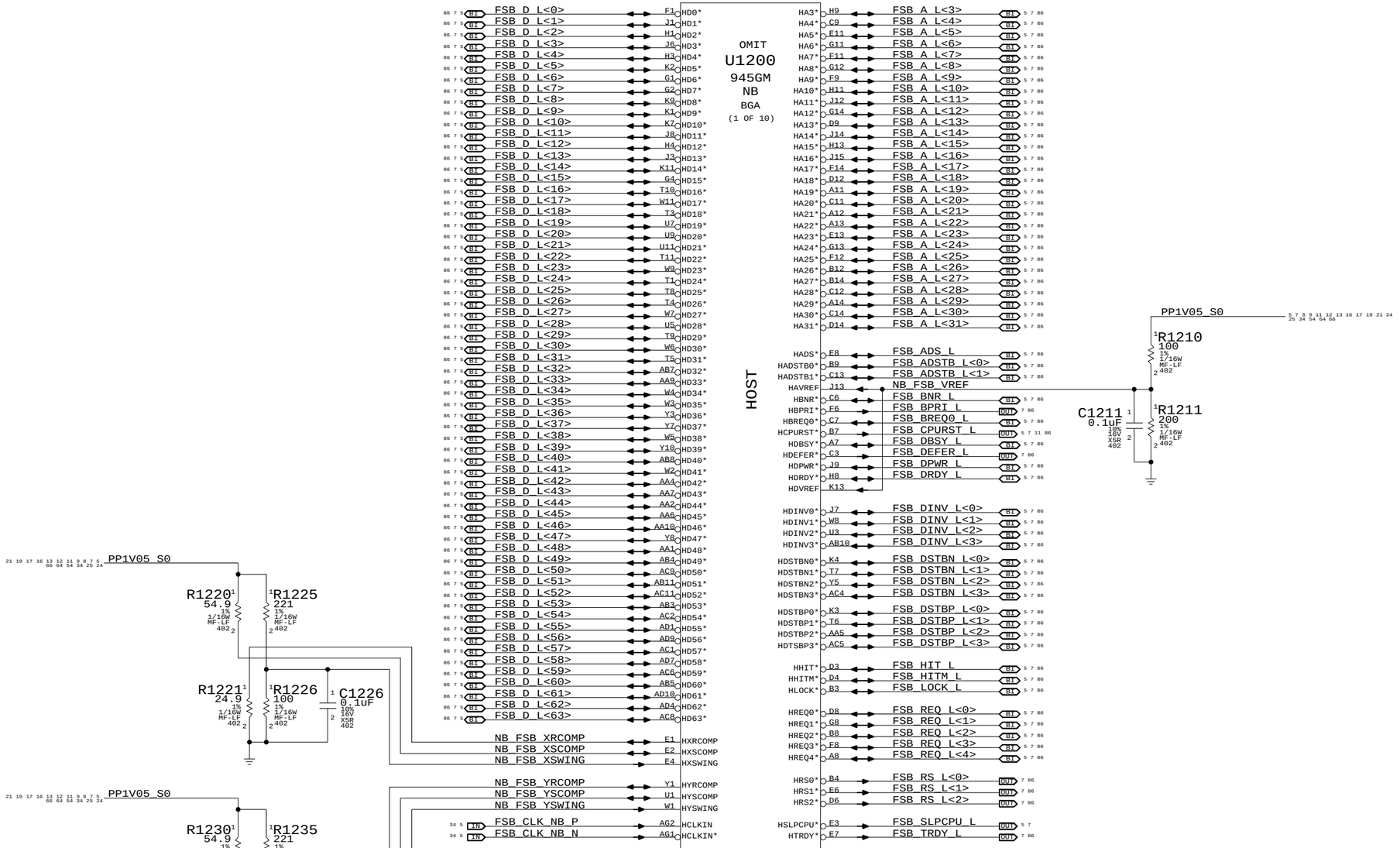

NB CPU Interface

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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

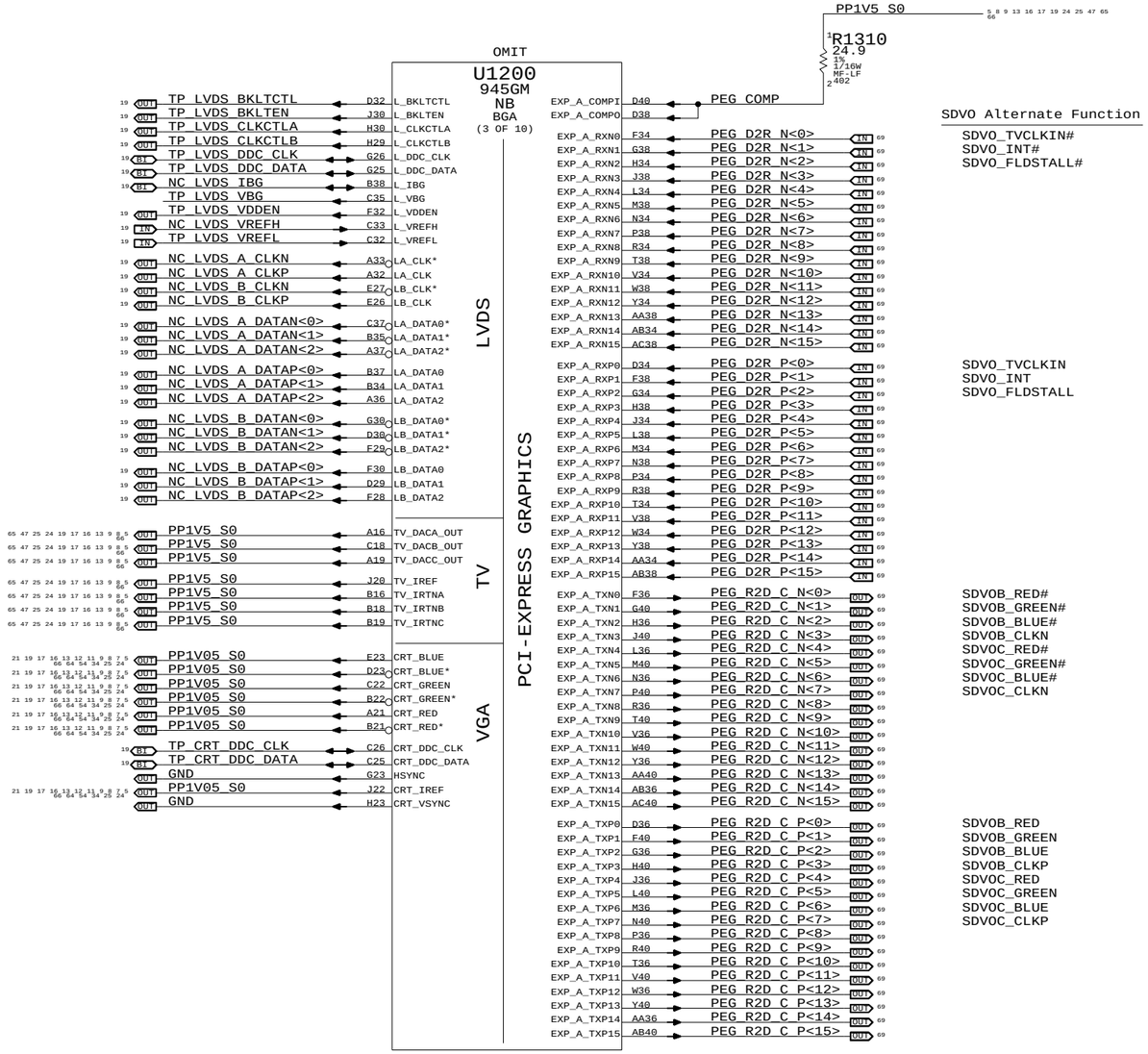
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail. Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces

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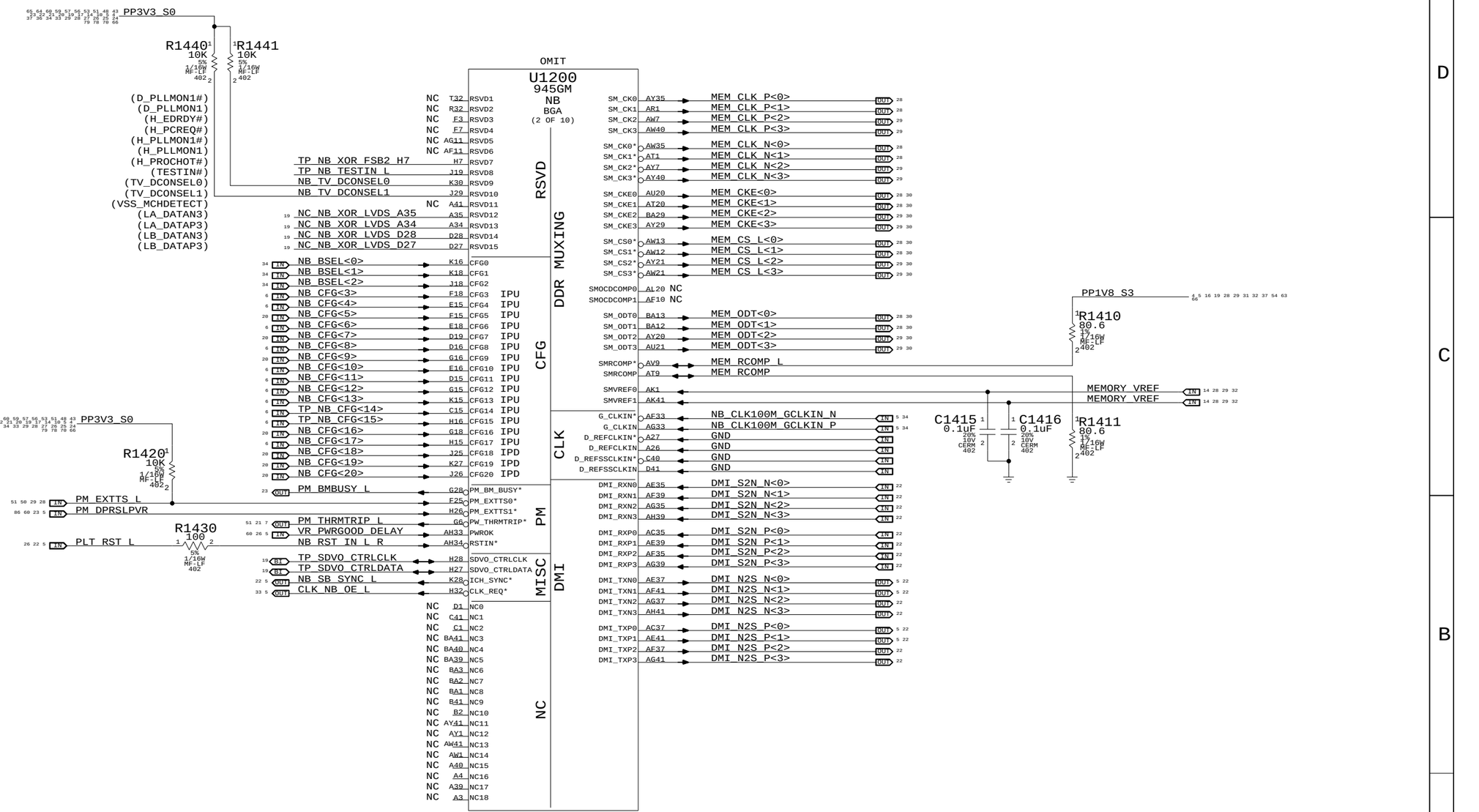

NB Misc Interfaces

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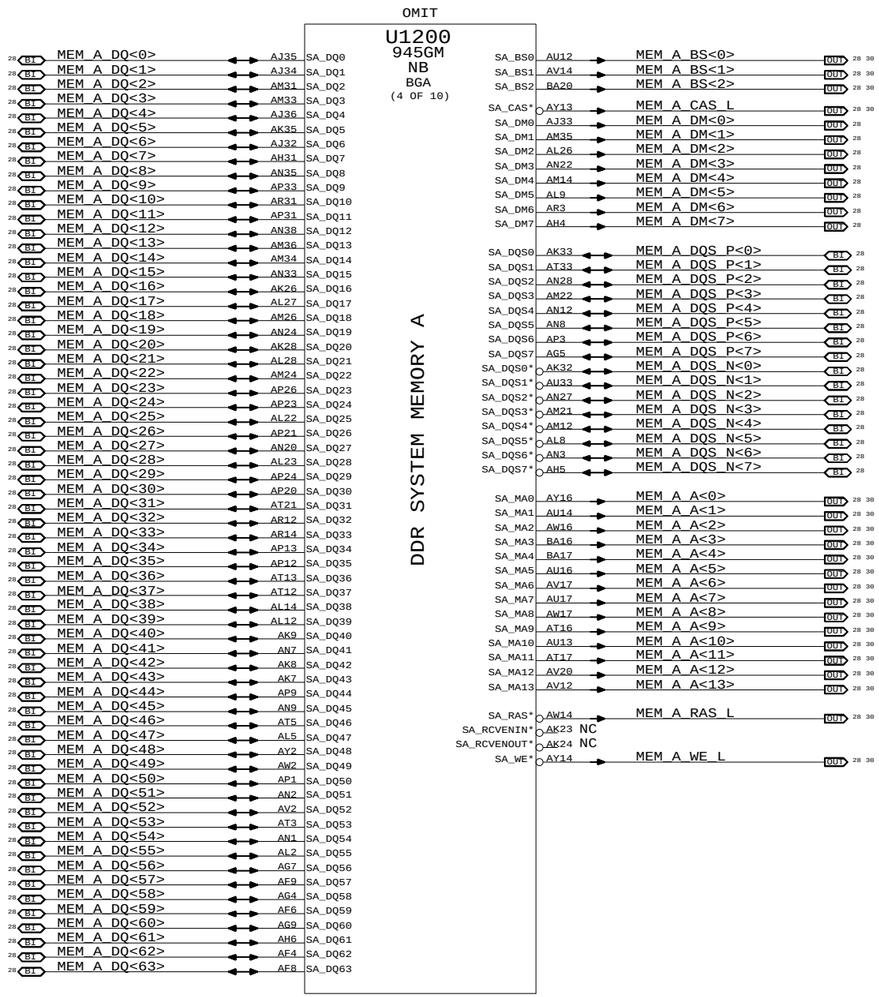

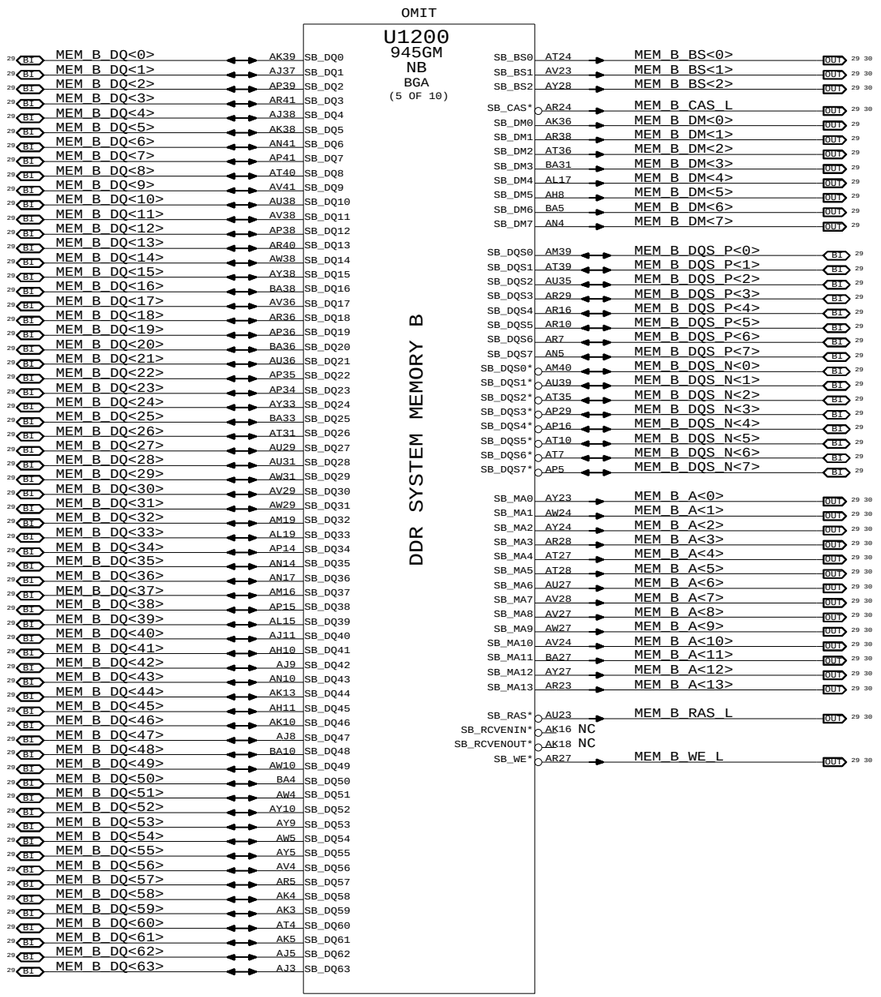

NB DDR2 Interfaces

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NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

PP1V05_S0

1.05V or 1.5V

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max

U1200 945GM NB BGA (6 OF 10) OMIT VCC

1.8V Max Current

Speed	1 Channel	2 Channel
400MTs	1300mA	2400mA
533MTs	1500mA	2800mA
667MTs	1700mA	3200mA

U1200 945GM NB BGA (7 OF 10) OMIT NCTF

PP1V5_S0

PP1V8_S3

NB_VCCSM_LF4
NB_VCCSM_LF5
NB_VCCSM_LF2
NB_VCCSM_LF1

C1614 0.47uF 20% 6.3V CERM-X5R 402

C1613 0.47uF 20% 6.3V CERM-X5R 402

C1615 0.47uF 20% 6.3V CERM-X5R 402
Layout Note: Place near pin BA23

C1620 10uF 20% 6.3V X5R 603
C1621 10uF 20% 6.3V X5R 603
C1610 0.47uF 20% 6.3V CERM-X5R 402
Layout Note: Place in cavity
Layout Note: Place near pin BA15

C1612 0.47uF 20% 6.3V CERM-X5R 402

C1611 0.47uF 20% 6.3V CERM-X5R 402

NB Power 1

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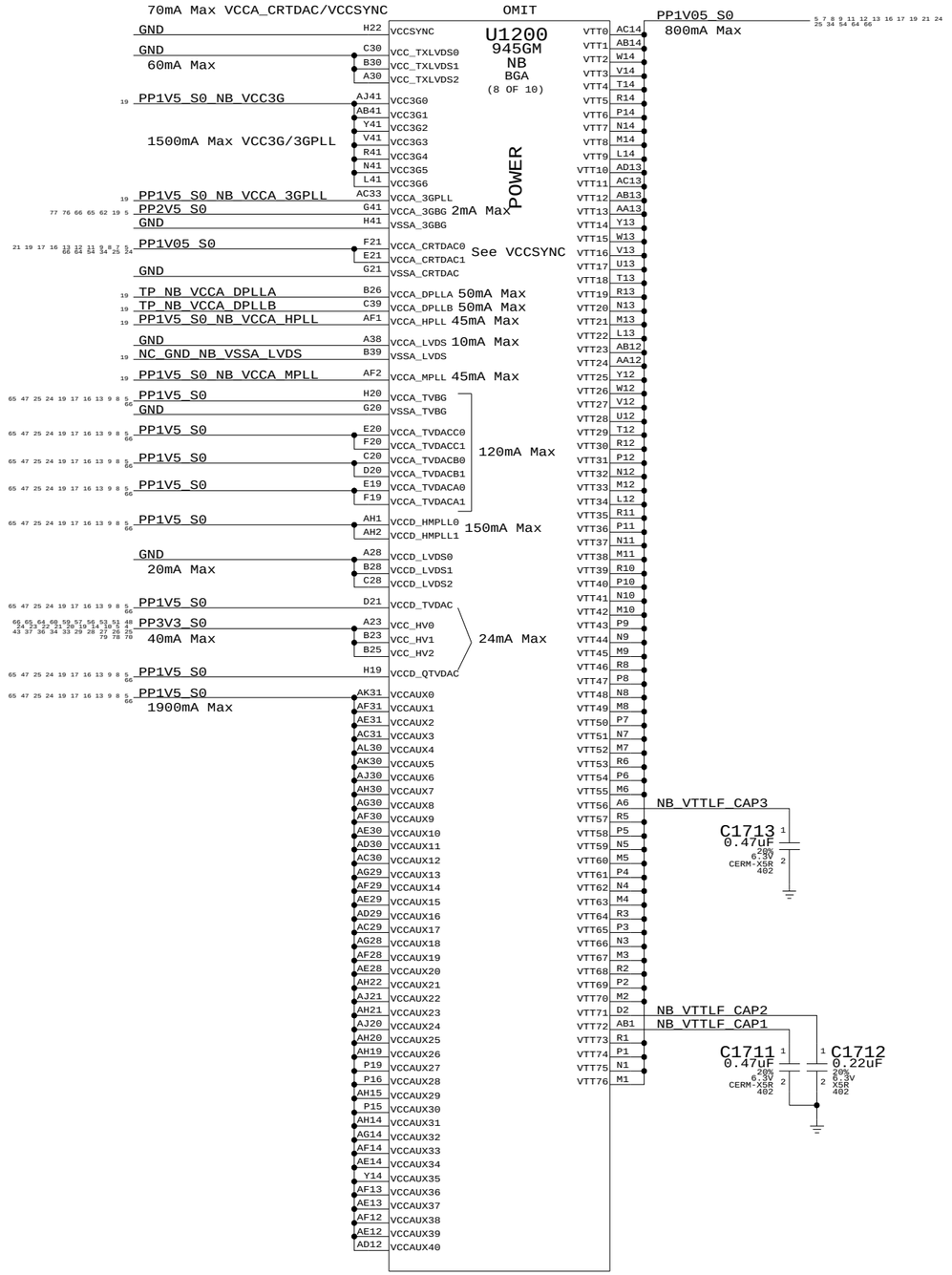

NB Power 2

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U1200
945GM
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VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

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U1200
945GM
NB
BGA
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VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE	SHT	OF
NONE	18	86

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Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	PP1V05_S0	1500mA Max
	PP1V05_S0	10mA Max?
	PP1V05_S0	800mA Max
	PP1V05_S0	?mA Max
3674mA Max	PP1V5_S0	?mA Max
	PP1V5_S0	1500mA Max
	PP1V5_S0	?mA Max
	PP1V5_S0	100mA Max
	PP1V5_S0	24mA Max
	PP1V5_S0	150mA Max
	PP1V5_S0	1900mA Max
3200mA Max	PP1V8_S3	3200mA Max
132mA Max	GND	70mA Max
	GND	60mA Max
	PP2V5_S0	2mA Max
40mA Max?	PP3V3_S0	?mA Max
	PP3V3_S0	40mA Max

PP1V05_S0 → PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, PP1V05_S0, GND, GND

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) → TP_CRT_DDC_CLK

TP_CRT_DDC_DATA (MAKE_BASE=TRUE) → TP_CRT_DDC_DATA

PP1V5_S0 → PP1V5_S0 ×8

TP_LVDS_BKLTCTL	TP_LVDS_BKLTCTL
TP_LVDS_BKLTEN	TP_LVDS_BKLTEN
TP_LVDS_CLKCTLA	TP_LVDS_CLKCTLA
TP_LVDS_CLKCTLB	TP_LVDS_CLKCTLB
TP_LVDS_DDC_CLK	TP_LVDS_DDC_CLK
TP_LVDS_DDC_DATA	TP_LVDS_DDC_DATA
NC_LVDS_IBG	NC_LVDS_IBG
TP_LVDS_VDDEN	TP_LVDS_VDDEN
NC_LVDS_VREFH	NC_LVDS_VREFH
TP_LVDS_VREFL	TP_LVDS_VREFL
NC_LVDS_A_CLKP	NC_LVDS_A_CLKP
NC_LVDS_A_CLKN	NC_LVDS_A_CLKN
NC_LVDS_A_DATAP<2..0>	LVDS_A_DATA_P<2..0>
NC_LVDS_A_DATAN<2..0>	LVDS_A_DATA_N<2..0>
NC_LVDS_B_CLKP	NC_LVDS_B_CLKP
NC_LVDS_B_CLKN	NC_LVDS_B_CLKN
NC_LVDS_B_DATAP<2..0>	LVDS_B_DATA_P<2..0>
NC_LVDS_B_DATAN<2..0>	LVDS_B_DATA_N<2..0>
NC_NB_XOR_LVDS_A34	NC_NB_XOR_LVDS_A34
NC_NB_XOR_LVDS_A35	NC_NB_XOR_LVDS_A35
NC_NB_XOR_LVDS_D27	NC_NB_XOR_LVDS_D27
NC_NB_XOR_LVDS_D28	NC_NB_XOR_LVDS_D28
TP_SDVO_CTRLCLK	TP_SDVO_CTRLCLK
TP_SDVO_CTRLDATA	TP_SDVO_CTRLDATA

(MCH LVDS DATA/CLK TX 2.5V PWR) → GND

(MCH LVDS DIGITAL 1.5V PWR) → GND

(MCH LVDS ANALOG 2.5V PWR) → GND

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) → NC_GND_NB_VSSA_LVDS

PP1V05_S0 → (MCH CRTDAC ANALOG 2.5V PWR) PP1V05_S0, GND

(MCH H/V SYNC 2.5V PWR) → GND

PP1V5_S0 → (MCH TVDAC DEDICATED PWR 1.5V) PP1V5_S0

(MCH TVDAC DIGITAL QUIET 1.5V PWR) → PP1V5_S0

(MCH TV OUT CHANNEL A 3.3V PWR) → PP1V5_S0

(MCH TV OUT CHANNEL B 3.3V PWR) → PP1V5_S0

(MCH TV OUT CHANNEL C 3.3V PWR) → PP1V5_S0

(MCH TV DAC BAND GAP 3.3V PWR) → PP1V5_S0

GND

TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) → (MCH DISPLAY A PLL 1.5V PWR) TP_NB_VCCA_DPLLA

TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) → (MCH DISPLAY B PLL 1.5V PWR) TP_NB_VCCA_DPLLB

GND ×4

PP1V05_S0 (1500mA Max) → GMCH CORE PWR 1.05V BYPASS

CRITICAL	C1902	C1903	C1904	C1905	C1906	C1907
C1900	10uF	10uF	1uF	0.22uF	0.22uF	0.22uF
470uF-9MOHM	20%	20%	10%	20%	20%	20%
20%	6.3V	6.3V	6.3V	6.3V	6.3V	6.3V
2.5V	X5R	X5R	CERM	X5R	X5R	X5R
POLY	0603	0603	402	402	402	402
D2TS						

PP1V05_S0 (800mA Max) → MCH VTT BYPASS (MCH FSB 1.05V PWR) (SHARE C0940 470UF)

C1965	C1966
4.7uF	2.2uF
20%	20%
6.3V	6.3V
CERM	CERM1
603	603

Layout Note: Place in cavity

C1967: 0.22uF, 20%, 6.3V, X5R, 402

Layout Note: Place on the edge

PP3V3_S0 (40mA Max) → MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)

C1914: 10uF, 20%, 6.3V, X5R, 603

C1915: 0.1uF, 20%, 10V, CERM, 402

PP2V5_S0 (2mA Max) → MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)

C1916: 0.1uF, 20%, 10V, CERM, 402

PP1V5_S0 (1900mA Max) → GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

C1918: 0.1uF, 20%, 10V, CERM, 402

PP1V5_S0 (100mA Max) → L1934 FERR-120-OHM-0.2A (0603) → GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR) PP1V5_S0_NB_VCCA_HPLL (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V) 45mA Max

C1934: 22UF, 20%, 6.3V, CERM, 805

C1935: 0.1uF, 20%, 10V, CERM, 402

PP1V5_S0 → L1936 FERR-120-OHM-0.2A (0603) → GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR) PP1V5_S0_NB_VCCA_MPLL (MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V) 45mA Max

C1936: 22UF, 20%, 6.3V, CERM, 805

C1937: 0.1uF, 20%, 10V, CERM, 402

PP1V5_S0 (1500mA Max) → L1970 91nH (1210)

Layout Note: Place L and C close to MCH

C1970: 220UF, 20%, 2.5V, POLY, SMB2

C1971: 10uF, 20%, 6.3V, X5R, 603

C1972: 10uF, 20%, 6.3V, X5R, 603

Layout Note: 10uF caps should be close to MCH on opposite side.

GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR) PP1V5_S0_NB_VCC3G (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V) → 1500mA Max

PP1V5_S0 → L1975 1.0UH-220MA-0.12-OHM (0805) → PP1V5_S0_NB_3GPLL_F (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.4 mm, VOLTAGE=1.5V)

R1975: 0.51, 1%, 1/16W, MF-LF, 402

C1975: 10uF, 20%, 6.3V, X5R, 603

C1976: 0.1uF, 20%, 10V, CERM, 402

GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR) PP1V5_S0_NB_VCCA_3GPLL (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.5V)

Layout Note: 3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

NB (GM) Decoupling

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NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
1 R2075
2.2K
5%
1/16W
MF-LF
2 402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
1 R2077
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
1 R2079
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
1 R2085
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<17>	RESERVED

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

PP3V3_S0
48,51,53,56,57,59,60,64,65,66
4,5,14,17,19,20,23,22,23,24
25,26,27,28,29,33,34,36,37,43
70,78,79
NBCFG_VCC_1V5
1 R2058
2.2K
5%
1/16W
MF-LF
2 402

14 NB_CFG<18>
Internal pull-down

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

PP3V3_S0
37,43,48,51,53,56,57,59,60,64
4,5,14,15,16,17,19,20,21,22,23,24
25,26,27,28,29,33,34,36
65,66,70,78,79
NBCFG_DMI_REVERSE
1 R2059
2.2K
5%
1/16W
MF-LF
2 402

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

PP3V3_S0
78,79
2,5,14,17,19,20,21,22,23,24
25,26,27,28,29,33
60,64,65,66,70
NBCFG_SDVO_AND_PCIE
1 R2060
2.2K
5%
1/16W
MF-LF
2 402

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

NB Config Straps

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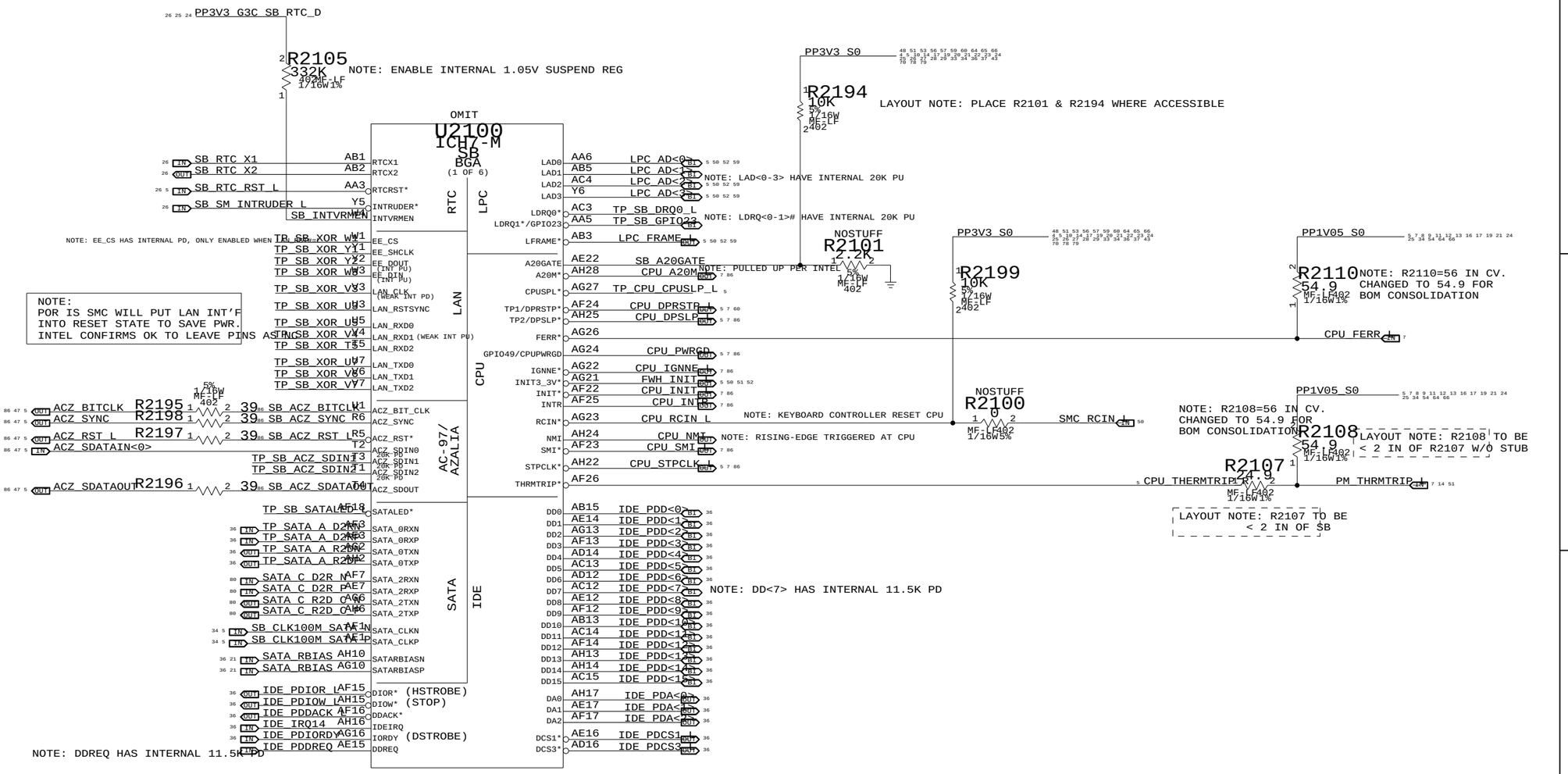

	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

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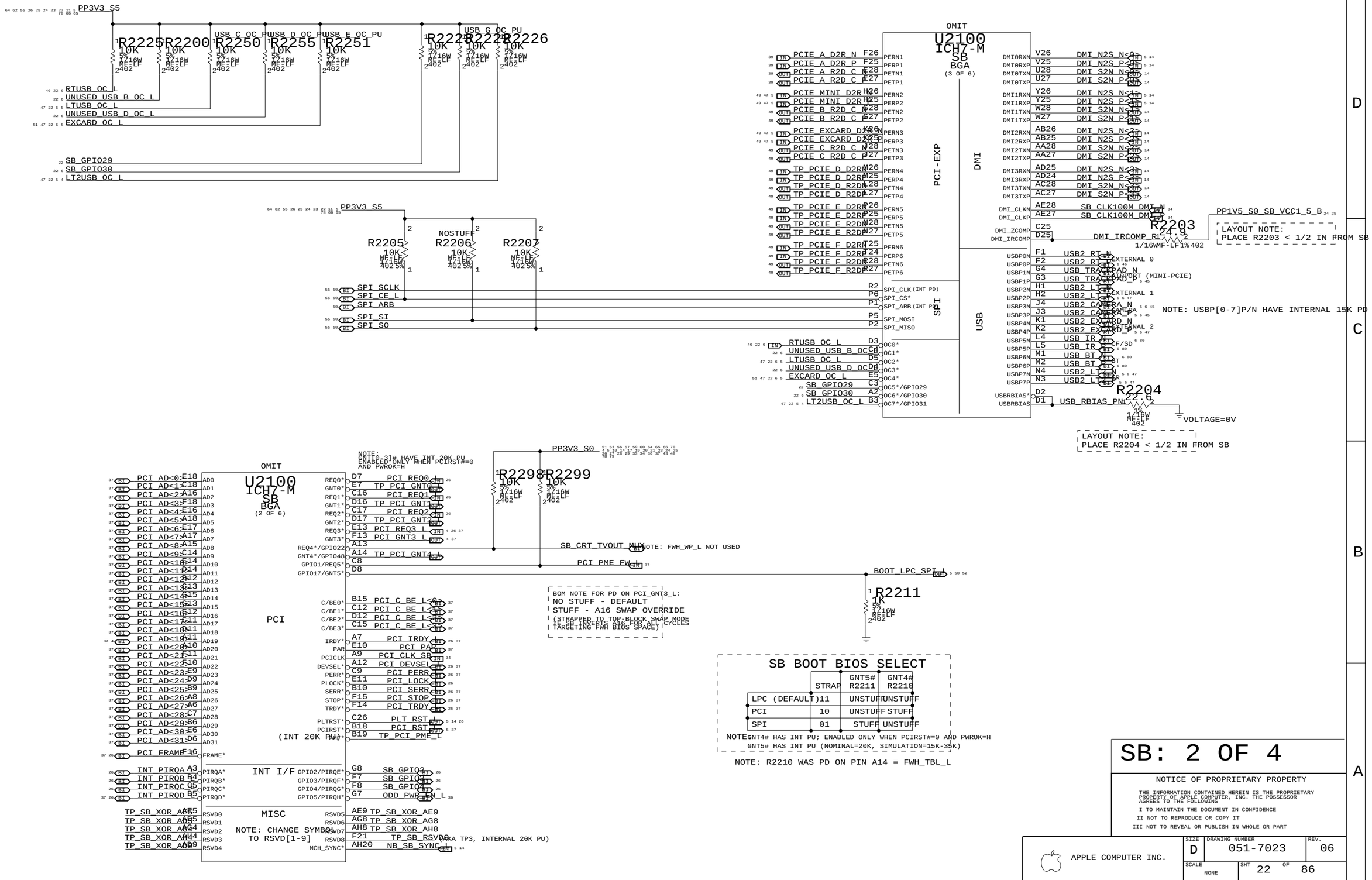

SB: 2 OF 4

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NONE	22	86

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NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

NO_REBOOT_MODE

PP3V3_S0

PP3V3_S5

RP2300 10K 5% 1/16W 5M-LF

R2318 10K 1/16W 402 2MF-LF 5%
R2395 8.2K 1/16W 402 2MF-LF 5%
R2396 10K 1/16W 402 2MF-LF 5%
R2397 8.2K 1/16W 402 2MF-LF 5%
R2327 10K 1/16W 402 2MF-LF 5%
R2326 10K 1/16W 402 2MF-LF 5%
R2323 1K 1/16W 402 2MF-LF 5%
NOSTUFF NOSTUFF

R2398 1K 1/16W 402 2MF-LF 5%
R2320 10K 1/16W 402 2MF-LF 5%
R2317 10K 1/16W 402 2MF-LF 5%
R2316 10K 1/16W 402 2MF-LF 5%

OMIT
U2100
ICH7-M SB
BGA
(4 OF 6)

SMBUS_SB_SCL
SMBUS_SB_SDA
SMB_LINK_ALERT_L
SMLINK<0>
SMLINK<1>
NOT USED
PM_RI_L
SB_SPKR
PM_SUS_STAT_L
PM_SYSRST_L
PM_BMBUSY_L
SMB_ALERT_L
NOTE: RESERVED FOR FUTURE

SMB: SMBCLK C22, SMBDATA B22, SMLINKALERT* A26, SMLINK0 B25, SMLINK1 A25
SPKR (INT WEAK PD) A19
SUS_STAT* A27
SYS_RST* A22
GPIO0/BM_BUSY* AB18
GPIO11/SMBALERT* B23

PM_STPPCI_L
PM_STPCPU_L
SB_GPIO26
BIOS_REC
FWH_MFG_MODE
PM_CLKRUN_L
TP_AZ_DOCK_EN
AZ_DOCK_RST_L
RESERVED FOR MOBILE AZALIA DOCKING INTF

GPIO18/STPPCI* AC20
GPIO20/STPCPU* AF21
GPIO26 A21
GPIO27 B21
GPIO28 E23
GPIO32/CLKRUN* AG18
GPIO33/AZ_DOCK_EN* AC19
GPIO34/AZ_DOCK_RST* U2

PCIE_WAKE_L
INT_SERIRQ
PM_THRM_L
VR_PWRGD_CK410
TP_SB_GPIO6
SMC_RUNTIME_SCI_L
SMC_EXTSMI_L

WAKE* F20
SERIRQ AH21
THRM* AF20
VRMPWRGD AD22
GPIO6 AG21
GPIO7 AC18
GPIO8 E21

SATA GPIO
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP

AF19 SB_GPIO21 100
AH18 SB_GPIO19 100
AH19
AE19 SB_GPIO37 100
R2302 R2303 R2305
SATA_C_DET_L

CLKS
CLK14 AC1 SB_CLK14P3M_TIMER
CLK48 B2 SB_CLK48M_USBCTLR
SUSCLK C20 TP_SB_SUS_CLK

PWR MNGT
SLP_S3* B24 PM_SLP_S3_L
SLP_S4* D23 PM_SLP_S4_L
SLP_S5* F22 PM_SLP_S5_L
PWROK AA4 PM_SB_PWROK
GPIO16/DPRSLPVR AC22 PM_DPRSLPVR
TP0/BATLOW* C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
PWRBTN* C23 PM_PWRBTN_L
LAN_RST* C19 PM_LAN_ENABLE NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* Y4

SYS GPIO
GPIO9 E20 SMS_INT_L
GPIO10 A20 SMC_SB_NMI
GPIO12 F19 PATA_PWR_EN
GPIO13 E19
GPIO14 R4 IDE_RESET_L
GPIO15 E22 SV_SET_UP
GPIO24 R3 CRB_SV_DET
GPIO25 D20 TP_SB_GPIO25_DO_NOT_USE
GPIO35 AD21 SB_CLK100M_SATA_OE_L
GPIO38 AD20 TP_SB_GPIO38
GPIO39 AE20 SATA_C_PWR_EN_L

DEF=GPI
DEF=GPI
OD
DEF=GPI

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

PP3V3_S5
R2319 10K 1/16W 402 2MF-LF 5%
R2343 8.2K 1/16W 402 2MF-LF 5%
PM_BATLOW_L
R2399 100K 1/16W 402 2MF-LF 5%
PM_RSMRST_L
SMC_WAKE_SCI_L

PP3V3_S5
R2306 R2308 10K 1/16W 402 2MF-LF 5%
NOSTUFF
SV_SET_UP
CRB_SV_DET

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

R2307 10K 1/16W 402 2MF-LF 5%
R2309 0 1/16W 402 2MF-LF 5%
NOSTUFF

PP3V3_S5
R2313 R2310 10K 1/16W 402 2MF-LF 5%
FWH_MFG_MODE
BIOS_REC

R2314 0 1/16W 402 2MF-LF 5%
R2311 10K 1/16W 402 2MF-LF 5%
NOSTUFF NOSTUFF

PP3V3_S5
R2390 10K 5% 1/16W MF-LF 2402
PATA_PWR_EN_L

PP3V3_S0
R2388 10K 5% 1/16W MF-LF 2402
SATA_C_PWR_EN_L

SB: 3 OF 4
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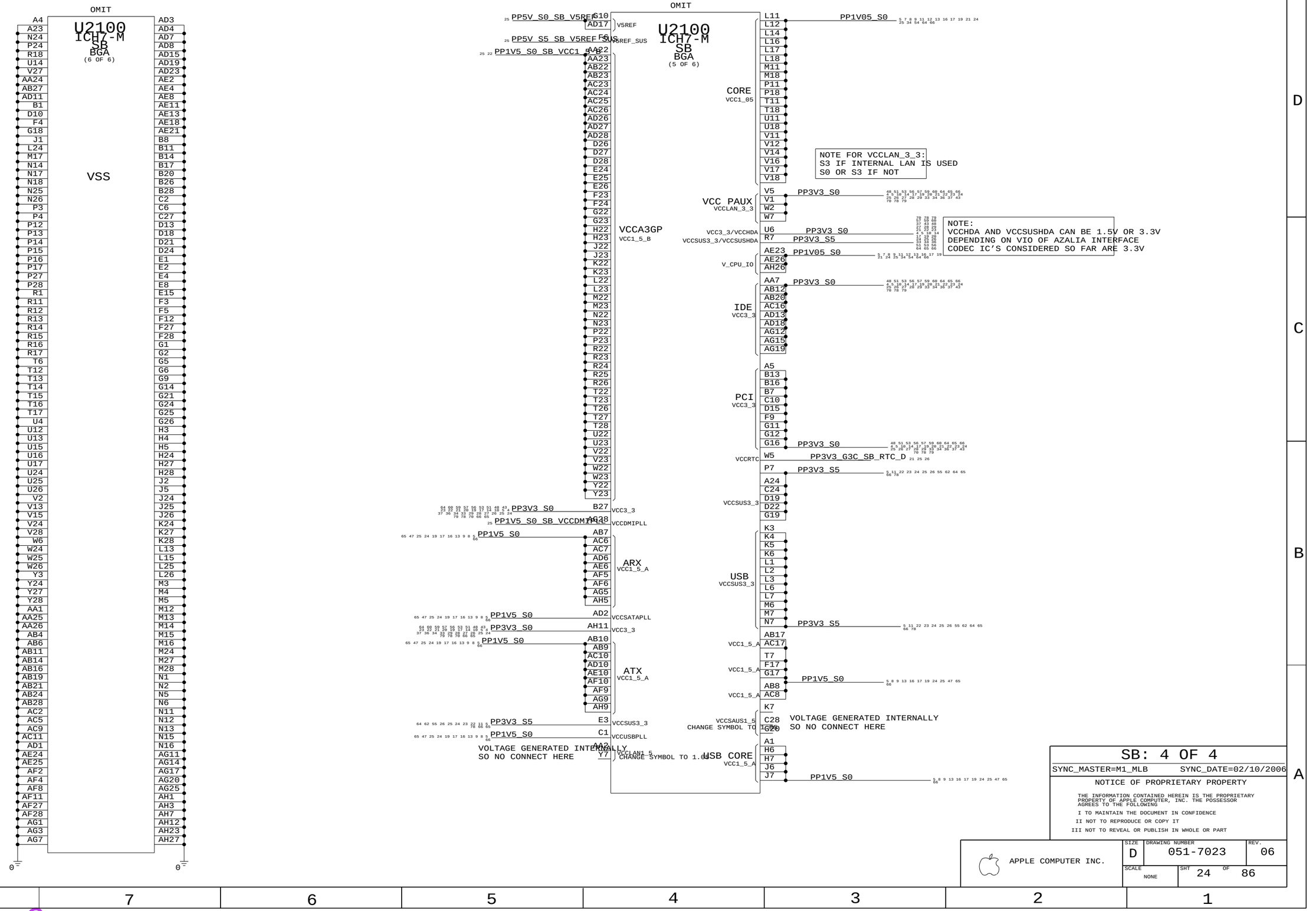

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8 | 7 | 6 | 5 | 4 | 3 | 2 | 1

PP3V3_S0
PP5V_S0
R2502 100 1/16W MF-LF 402 5%
D2502 BAT54DW SOT-363
ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2503 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
PP1V5_S0
C2511 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5

ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
PP1V5_S0
C2517 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2

PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
PP1V05_S0
C2518 0.1UF 10% 16V X5R 402
C2502 1UF 10% 6.3V CERM 402
C2516 330UF 20% 2.5V POLY CASE-C2
PLACEHOLDER FOR 270UF

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PP3V3_S5
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF 2531
C2531 0.1UF 10% 16V X5R 402
C2534 0.1UF 10% 16V X5R 402

PP3V3_S5
PP5V_S5
R2501 10 1/16W MF-LF 402 5%
D2502 BAT54DW SOT-363
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PP5V_S5_SB_V5REF_SUS
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2504 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PP3V3_S0
C2513 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11

PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS W1,
V5, W2, OR W7
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
PP3V3_S0
C2519 0.1UF 10% 16V X5R 402

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
PP3V3_S5
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
C2533 0.1UF 10% 16V X5R 402
C2532 0.1UF 10% 16V X5R 402

ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
PP1V5_S0
C2514 1UF 10% 6.3V CERM 402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9

ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
PP3V3_S0
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
C2521 0.1UF 10% 16V X5R 402

ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
PP1V5_S0
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
C2510 0.1UF 10% 16V X5R 402

PP1V5_S0
L2500 100-OHM-EMI SM-3
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2500 270UF 20% 2.5V POLY SMB2
C2505 0.1UF 10% 16V X5R 402
C2506 0.1UF 10% 16V X5R 402
C2507 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PP3V3_S5
C2520 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
PP1V05_S0
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
C2523 0.1UF 10% 16V X5R 402
C2522 0.1UF 10% 16V X5R 402
C2524 4.7UF 20% 6.3V CERM 603

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
PP1V5_S0
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1 ...
C2512 1UF 10% 6.3V CERM 402

ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
PP1V5_S0
C2515 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PP3V3_S0
C2509 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB

ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
PP3V3_S0
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7
C2525 0.1UF 10% 16V X5R 402

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
PP3V3_S0
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
C2526 0.1UF 10% 16V X5R 402
C2527 0.1UF 10% 16V X5R 402
C2528 0.1UF 10% 16V X5R 402

PP1V5_S0
R2500 1/10W5% MF-LF603
L2507 0.28-OHM 1206
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
PP1V5_S0_SB_VCCDMIPLL
C2501 0.01UF 10% 16V CERM 402
C2508 10UF 20% 6.3V X5R 603
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
PP3V3_G3C_SB_RTC_D
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
C2530 0.1UF 10% 16V X5R 402
C2529 0.1UF 10% 16V X5R 402

SB: 4 OF 4

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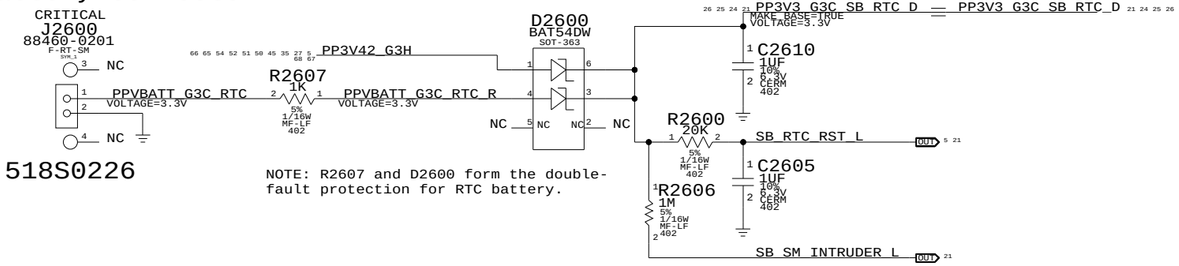
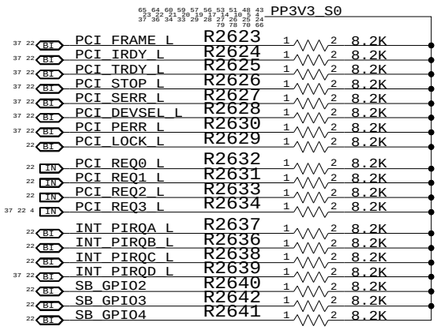
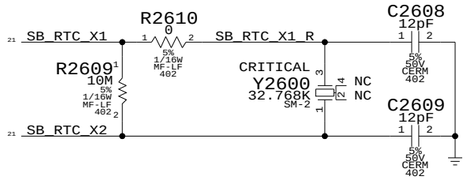
RTC Battery Connector

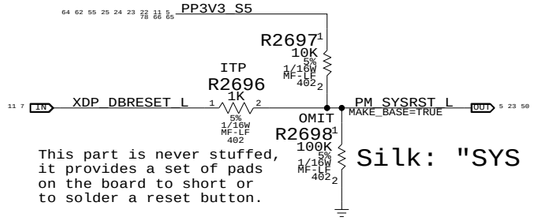


NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit



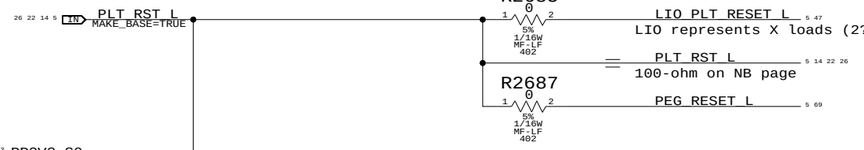


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

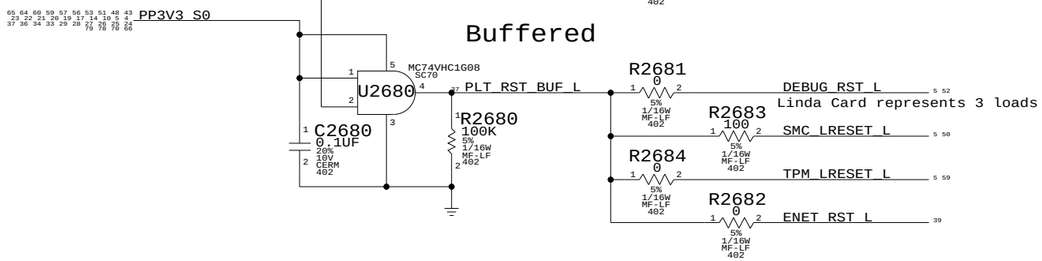
Silk: "SYS RST"

Platform Reset Connections

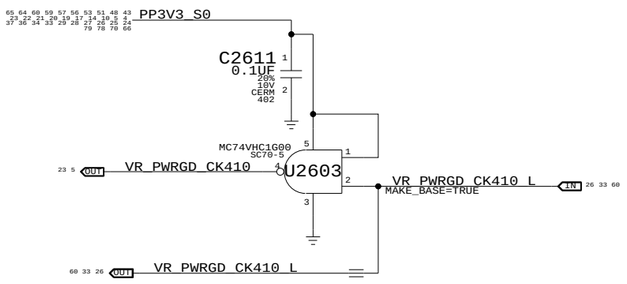
Unbuffered



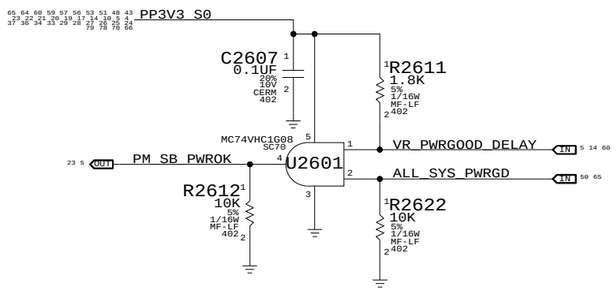
Buffered



Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



SB Misc

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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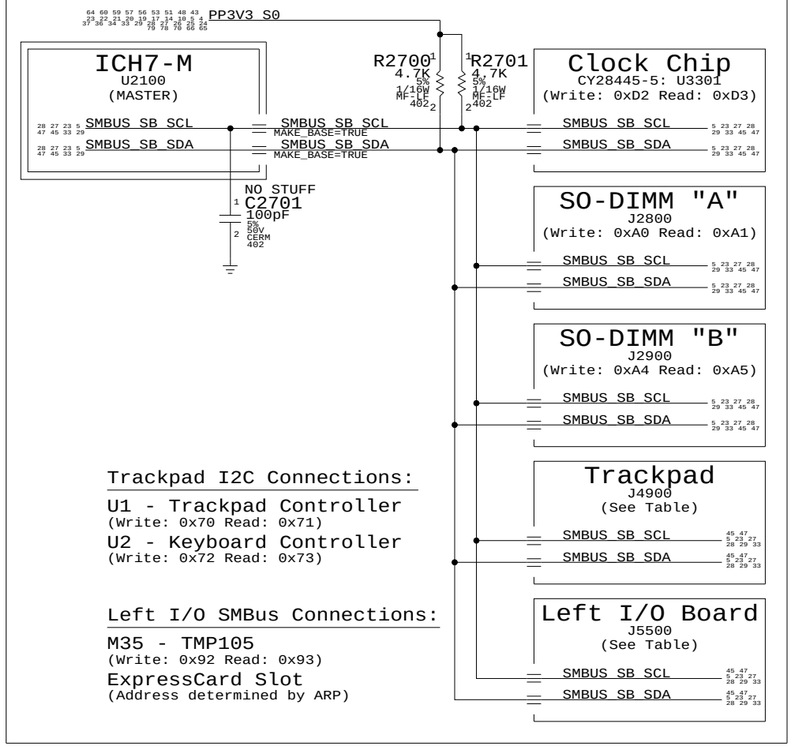
ICH7-M SMBus Connections



Trackpad I2C Connections:

U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

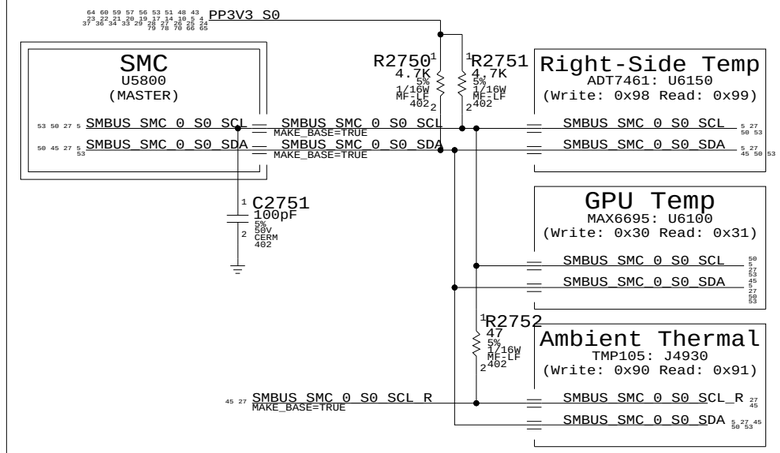
U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

Left I/O SMBus Connections:

M35 - TMP105
(Write: 0x92 Read: 0x93)

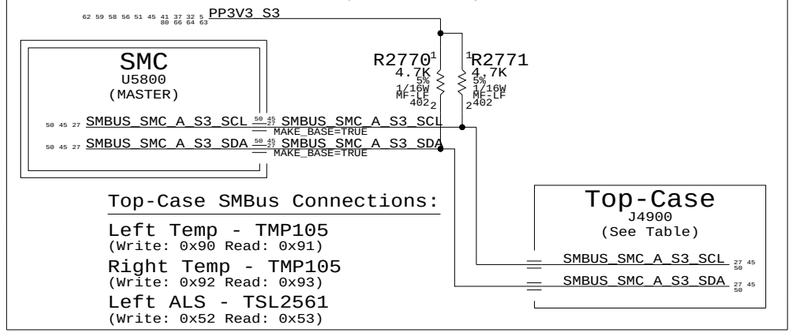
ExpressCard Slot
(Address determined by ARP)

SMC "0" SMBus Connections



SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



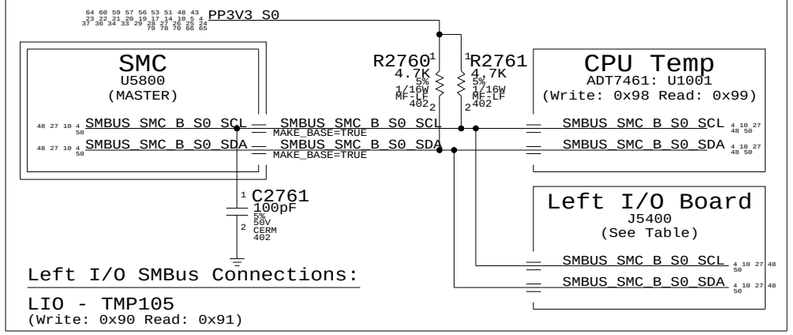
Top-Case SMBus Connections:

Left Temp - TMP105
(Write: 0x90 Read: 0x91)

Right Temp - TMP105
(Write: 0x92 Read: 0x93)

Left ALS - TSL2561
(Write: 0x52 Read: 0x53)

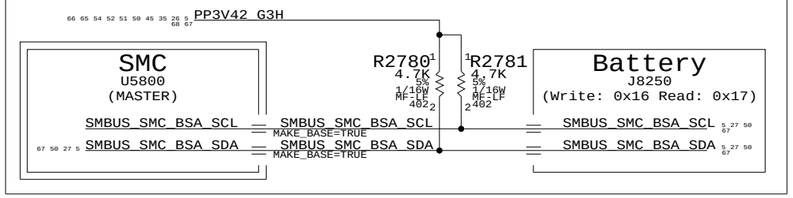
SMC "B" SMBus Connections



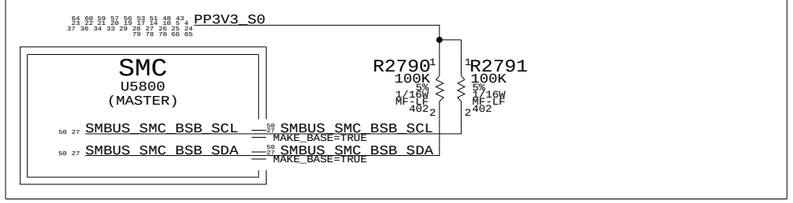
Left I/O SMBus Connections:

LIO - TMP105
(Write: 0x90 Read: 0x91)

SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=M1_MLB SYNC_DATE=01/04/2006

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Page Notes

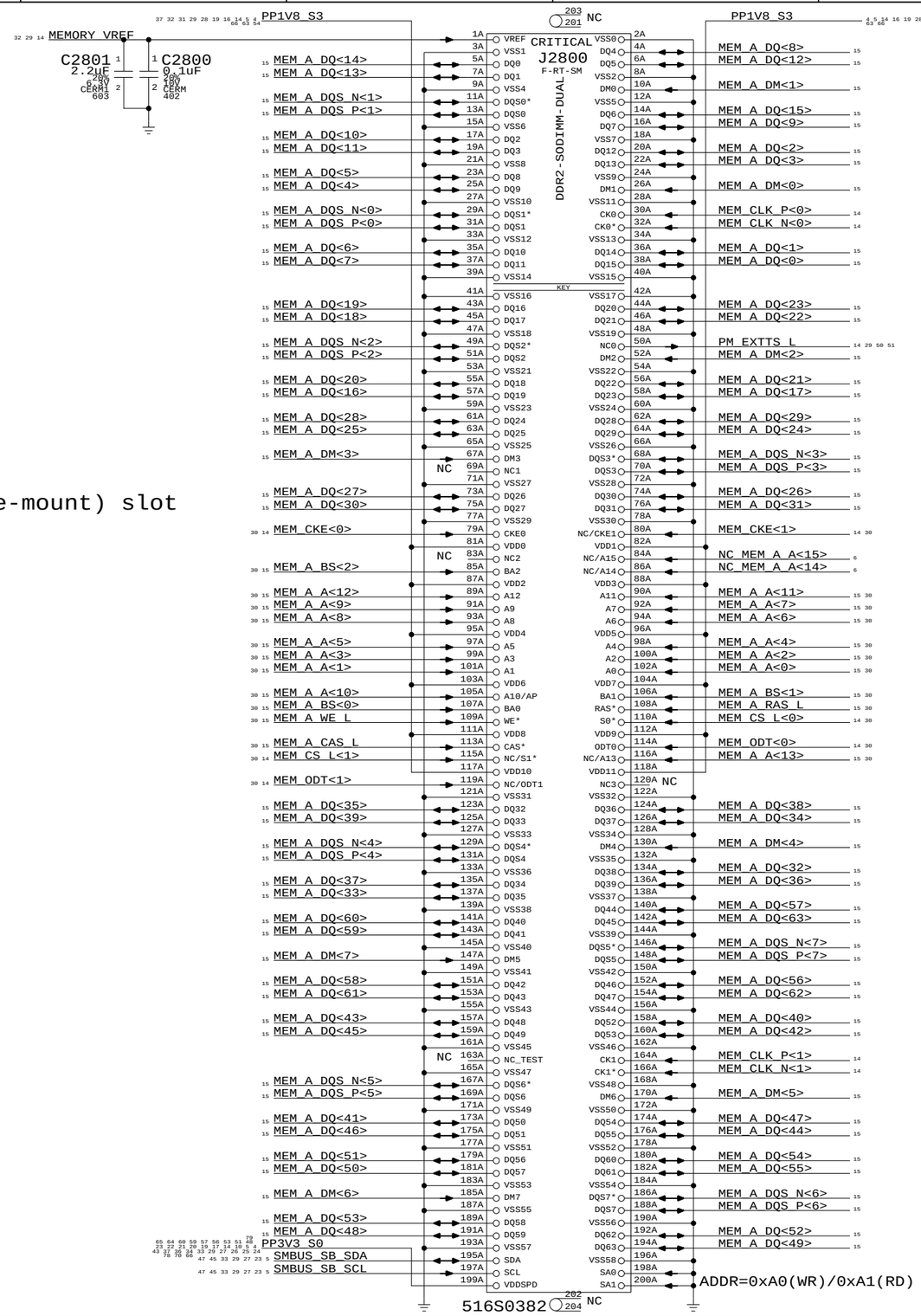
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

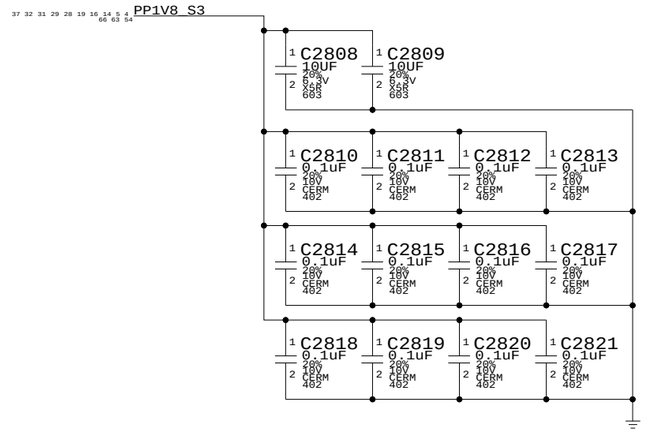
NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (surface-mount) slot



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7023	06

SCALE: NONE SHT 28 OF 86

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Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Upper" (thru-hole) slot

MEMORY_VREF

C2901 2.2uF 20% 6.3V CERM 603

C2900 0.1uF 20% 10V CERM 402

PP1V8_S3

CRITICAL
J2900
F-RT-TH1
DDR2-SODIMM-DUAL

	1B	VREF		2B	VSS0		
	3B	VSS1		4B	DQ4	MEM_B_DQ<9>	15
15 MEM_B_DQ<15>	5B	DQ0		6B	DQ5	MEM_B_DQ<11>	15
15 MEM_B_DQ<14>	7B	DQ1		8B	VSS2		
	9B	VSS4		10B	DM0	MEM_B_DM<1>	15
15 MEM_B_DQS_N<1>	11B	DQS0*		12B	VSS5		
15 MEM_B_DQS_P<1>	13B	DQS0		14B	DQ6	MEM_B_DQ<12>	15
	15B	VSS6		16B	DQ7	MEM_B_DQ<8>	15
15 MEM_B_DQ<10>	17B	DQ2		18B	VSS7		
15 MEM_B_DQ<13>	19B	DQ3		20B	DQ12	MEM_B_DQ<3>	15
	21B	VSS8		22B	DQ13	MEM_B_DQ<6>	15
15 MEM_B_DQ<7>	23B	DQ8		24B	VSS9		
15 MEM_B_DQ<2>	25B	DQ9		26B	DM1	MEM_B_DM<0>	15
	27B	VSS10		28B	VSS11		
15 MEM_B_DQS_N<0>	29B	DQS1*		30B	CK0	MEM_CLK_P<3>	14
15 MEM_B_DQS_P<0>	31B	DQS1		32B	CK0*	MEM_CLK_N<3>	14
	33B	VSS12		34B	VSS13		
15 MEM_B_DQ<1>	35B	DQ10		36B	DQ14	MEM_B_DQ<0>	15
15 MEM_B_DQ<4>	37B	DQ11		38B	DQ15	MEM_B_DQ<5>	15
	39B	VSS14		40B	VSS15		
		KEY					
	41B	VSS16		42B	VSS17		
15 MEM_B_DQ<21>	43B	DQ16		44B	DQ20	MEM_B_DQ<22>	15
15 MEM_B_DQ<19>	45B	DQ17		46B	DQ21	MEM_B_DQ<18>	15
	47B	VSS18		48B	VSS19		
15 MEM_B_DQS_N<2>	49B	DQS2*		50B	NC0	PM_EXTTS_L	14 28 50 51
15 MEM_B_DQS_P<2>	51B	DQS2		52B	DM2	MEM_B_DM<2>	15
	53B	VSS21		54B	VSS22		
15 MEM_B_DQ<20>	55B	DQ18		56B	DQ22	MEM_B_DQ<17>	15
15 MEM_B_DQ<23>	57B	DQ19		58B	DQ23	MEM_B_DQ<16>	15
	59B	VSS23		60B	VSS24		
15 MEM_B_DQ<29>	61B	DQ24		62B	DQ28	MEM_B_DQ<26>	15
15 MEM_B_DQ<24>	63B	DQ25		64B	DQ29	MEM_B_DQ<28>	15
	65B	VSS25		66B	VSS26		
15 MEM_B_DM<3>	67B	DM3		68B	DQS3*	MEM_B_DQS_N<3>	15
NC	69B	NC1		70B	DQS3	MEM_B_DQS_P<3>	15
	71B	VSS27		72B	VSS28		
15 MEM_B_DQ<27>	73B	DQ26		74B	DQ30	MEM_B_DQ<31>	15
15 MEM_B_DQ<25>	75B	DQ27		76B	DQ31	MEM_B_DQ<30>	15
	77B	VSS29		78B	VSS30		
30 14 MEM_CKE<2>	79B	CKE0		80B	NC/CKE1	MEM_CKE<3>	14 30
	81B	VDD0		82B	VDD1		
NC	83B	NC2		84B	NC/A15	NC_MEM_B_A<15>	6
30 15 MEM_B_BS<2>	85B	BA2		86B	NC/A14	NC_MEM_B_A<14>	6
	87B	VDD2		88B	VDD3		
30 15 MEM_B_A<12>	89B	A12		90B	A11	MEM_B_A<11>	15 30
30 15 MEM_B_A<9>	91B	A9		92B	A7	MEM_B_A<7>	15 30
30 15 MEM_B_A<8>	93B	A8		94B	A6	MEM_B_A<6>	15 30
	95B	VDD4		96B	VDD5		
30 15 MEM_B_A<5>	97B	A5		98B	A4	MEM_B_A<4>	15 30
30 15 MEM_B_A<3>	99B	A3		100B	A2	MEM_B_A<2>	15 30
30 15 MEM_B_A<1>	101B	A1		102B	A0	MEM_B_A<0>	15 30
	103B	VDD6		104B	VDD7		
30 15 MEM_B_A<10>	105B	A10/AP		106B	BA1	MEM_B_BS<1>	15 30
30 15 MEM_B_BS<0>	107B	BA0		108B	RAS*	MEM_B_RAS_L	15 30
30 15 MEM_B_WE_L	109B	WE*		110B	S0*	MEM_CS_L<2>	14 30
	111B	VDD8		112B	VDD9		
30 15 MEM_B_CAS_L	113B	CAS*		114B	ODT0	MEM_ODT<2>	14 30
30 14 MEM_CS_L<3>	115B	NC/S1*		116B	NC/A13	MEM_B_A<13>	15 30
	117B	VDD10		118B	VDD11		
30 14 MEM_ODT<3>	119B	NC/ODT1		120B	NC3	NC	
	121B	VSS31		122B	VSS32		
15 MEM_B_DQ<36>	123B	DQ32		124B	DQ36	MEM_B_DQ<32>	15
15 MEM_B_DQ<33>	125B	DQ33		126B	DQ37	MEM_B_DQ<37>	15
	127B	VSS33		128B	VSS34		
15 MEM_B_DQS_N<4>	129B	DQS4*		130B	DM4	MEM_B_DM<4>	15
15 MEM_B_DQS_P<4>	131B	DQS4		132B	VSS35		
	133B	VSS36		134B	DQ38	MEM_B_DQ<38>	15
15 MEM_B_DQ<34>	135B	DQ34		136B	DQ39	MEM_B_DQ<39>	15
15 MEM_B_DQ<35>	137B	DQ35		138B	VSS37		
	139B	VSS38		140B	DQ44	MEM_B_DQ<44>	15
15 MEM_B_DQ<40>	141B	DQ40		142B	DQ45	MEM_B_DQ<45>	15
15 MEM_B_DQ<41>	143B	DQ41		144B	VSS39		
	145B	VSS40		146B	DQS5*	MEM_B_DQS_N<5>	15
15 MEM_B_DM<5>	147B	DM5		148B	DQS5	MEM_B_DQS_P<5>	15
	149B	VSS41		150B	VSS42		
15 MEM_B_DQ<42>	151B	DQ42		152B	DQ46	MEM_B_DQ<46>	15
15 MEM_B_DQ<43>	153B	DQ43		154B	DQ47	MEM_B_DQ<47>	15
	155B	VSS43		156B	VSS44		
15 MEM_B_DQ<62>	157B	DQ48		158B	DQ52	MEM_B_DQ<58>	15
15 MEM_B_DQ<59>	159B	DQ49		160B	DQ53	MEM_B_DQ<63>	15
	161B	VSS45		162B	VSS46		
NC	163B	NC_TEST		164B	CK1	MEM_CLK_P<2>	14
	165B	VSS47		166B	CK1*	MEM_CLK_N<2>	14
15 MEM_B_DQS_N<7>	167B	DQS6*		168B	VSS48		
15 MEM_B_DQS_P<7>	169B	DQS6		170B	DM6	MEM_B_DM<7>	15
	171B	VSS49		172B	VSS50		
15 MEM_B_DQ<60>	173B	DQ50		174B	DQ54	MEM_B_DQ<56>	15
15 MEM_B_DQ<61>	175B	DQ51		176B	DQ55	MEM_B_DQ<57>	15
	177B	VSS51		178B	VSS52		
15 MEM_B_DQ<54>	179B	DQ56		180B	DQ60	MEM_B_DQ<55>	15
15 MEM_B_DQ<51>	181B	DQ57		182B	DQ61	MEM_B_DQ<50>	15
	183B	VSS53		184B	VSS54		
15 MEM_B_DM<6>	185B	DM7		186B	DQS7*	MEM_B_DQS_N<6>	15
	187B	VSS55		188B	DQS7	MEM_B_DQS_P<6>	15
15 MEM_B_DQ<52>	189B	DQ58		190B	VSS56		
15 MEM_B_DQ<49>	191B	DQ59		192B	DQ62	MEM_B_DQ<53>	15
PP3V3_S0	193B	VSS57		194B	DQ63	MEM_B_DQ<48>	15
SMBUS_SB_SDA	195B	SDA		196B	VSS58		
SMBUS_SB_SCL	197B	SCL		198B	SA0		
	199B	VDDSPD		200B	SA1		

516-0140

202 NC

20 NC

Resistor prevents pwr-gnd short

SODIMM_A_SA1
ADDR=0xA4(WR)/0xA5(RD)

PP3V3_S0

R2900 10K 5% 1/16W MF-LF 402

DDR2 Bypass Caps

(For return current)

PP1V8_S3

C2908 10UF 20% 6.3V X5R 603

C2909 10UF 20% 6.3V X5R 603

C2910 0.1uF 20% 10V CERM 402

C2911 0.1uF 20% 10V CERM 402

C2912 0.1uF 20% 10V CERM 402

C2913 0.1uF 20% 10V CERM 402

C2914 0.1uF 20% 10V CERM 402

C2915 0.1uF 20% 10V CERM 402

C2916 0.1uF 20% 10V CERM 402

C2917 0.1uF 20% 10V CERM 402

C2918 0.1uF 20% 10V CERM 402

C2919 0.1uF 20% 10V CERM 402

C2920 0.1uF 20% 10V CERM 402

C2921 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE	SHT	OF
NONE	29	86

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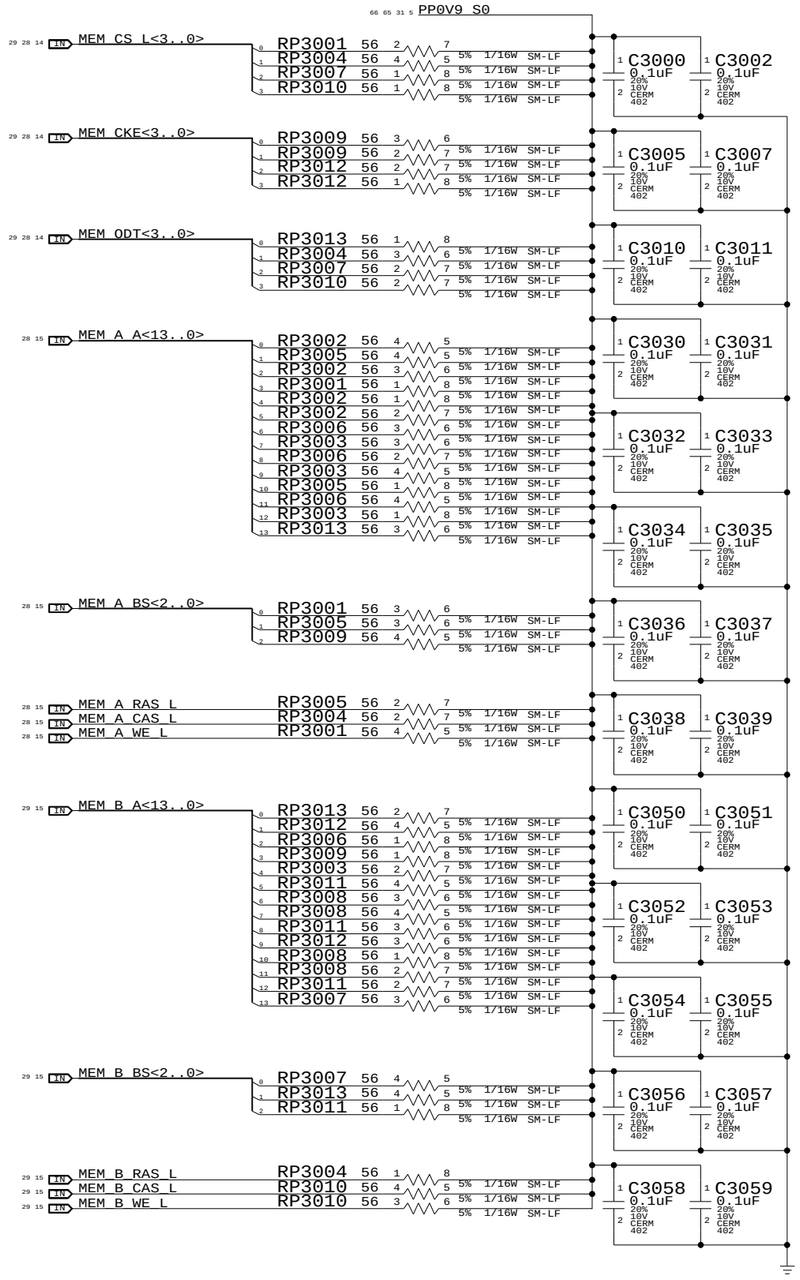
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/07/2006)

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SCALE NONE

SHT 30 OF 86

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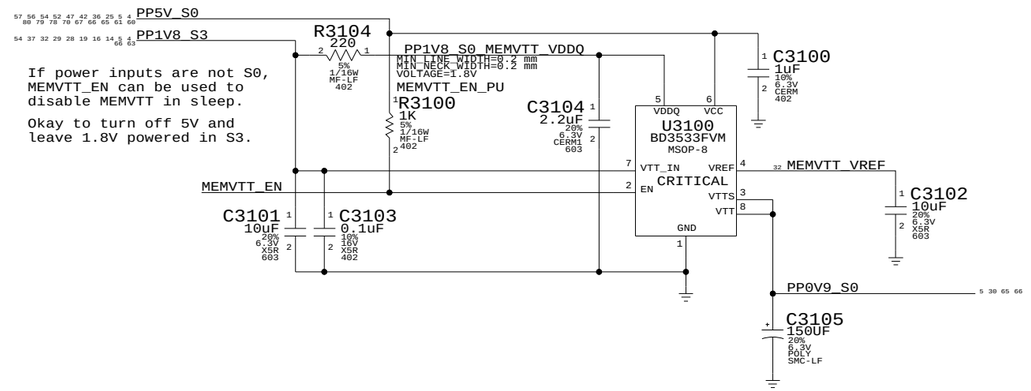
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE: NONE

SHT 31 OF 86

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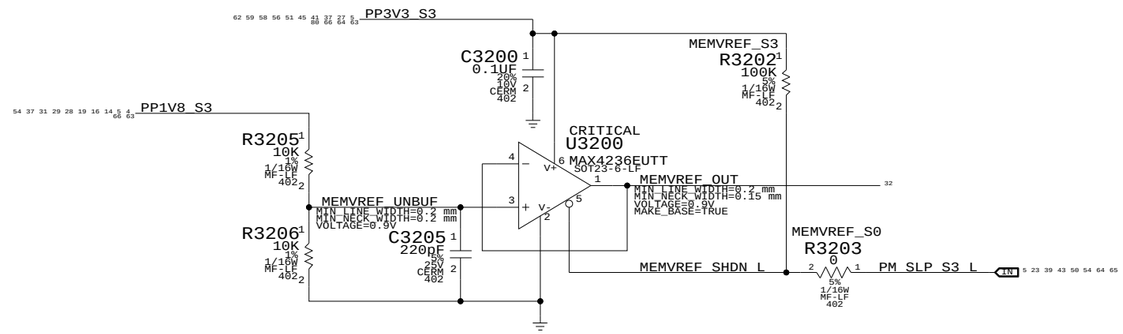

DDR2 VRef

SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

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SCALE	SHT	OF
NONE	32	86

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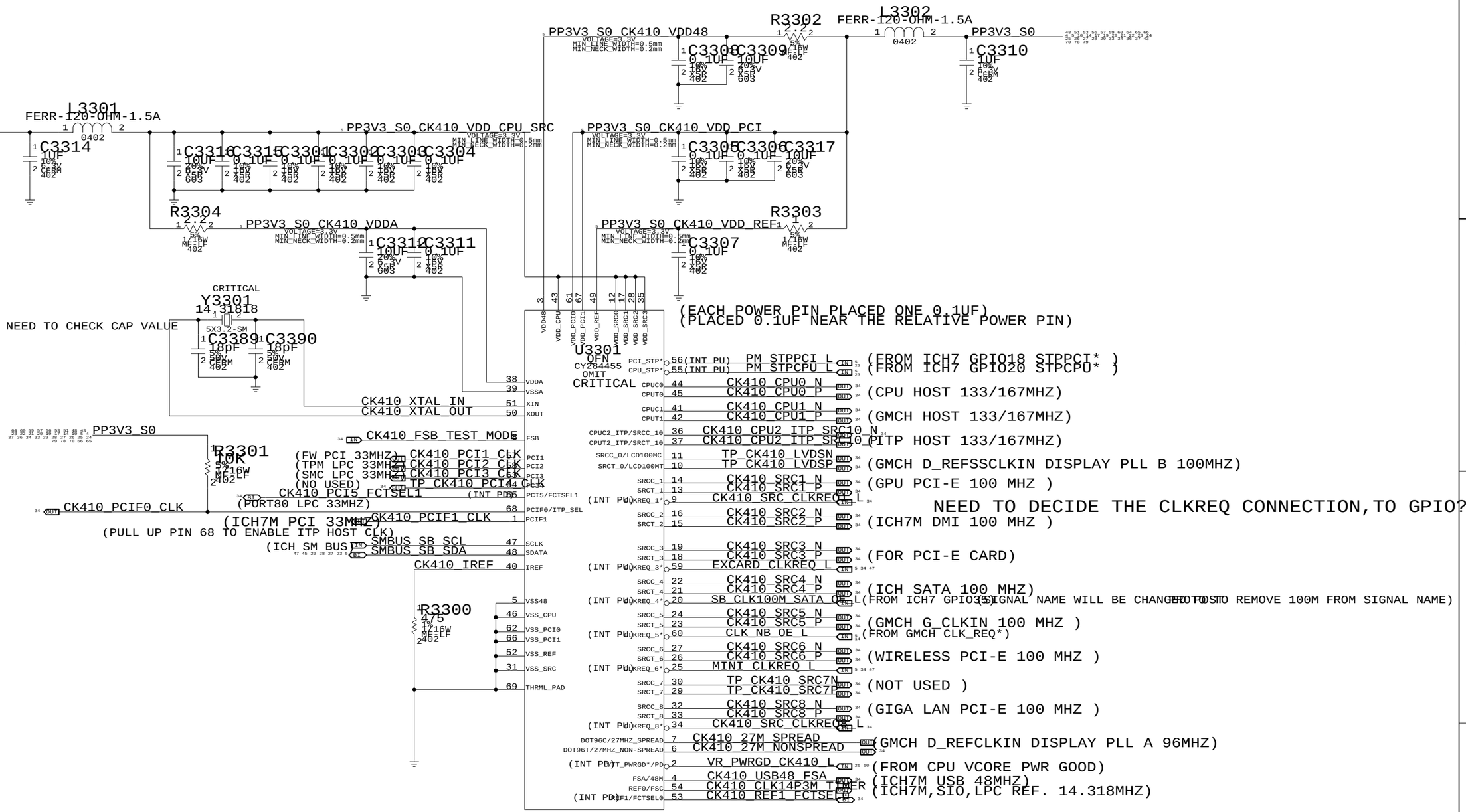

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SS	T100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF	LOW	BD	SRCT0	SRCC0

CLOCKS

SYNC_MASTER=MS_NCB SYNC_DATE=02/10/2006

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SCALE: NONE SHT 33 OF 86

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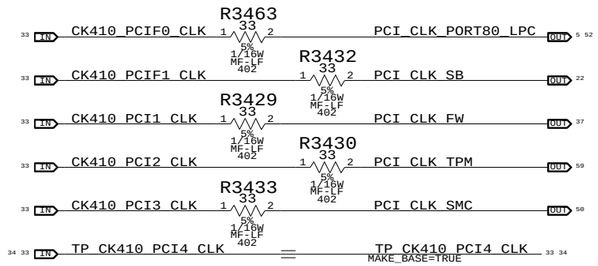

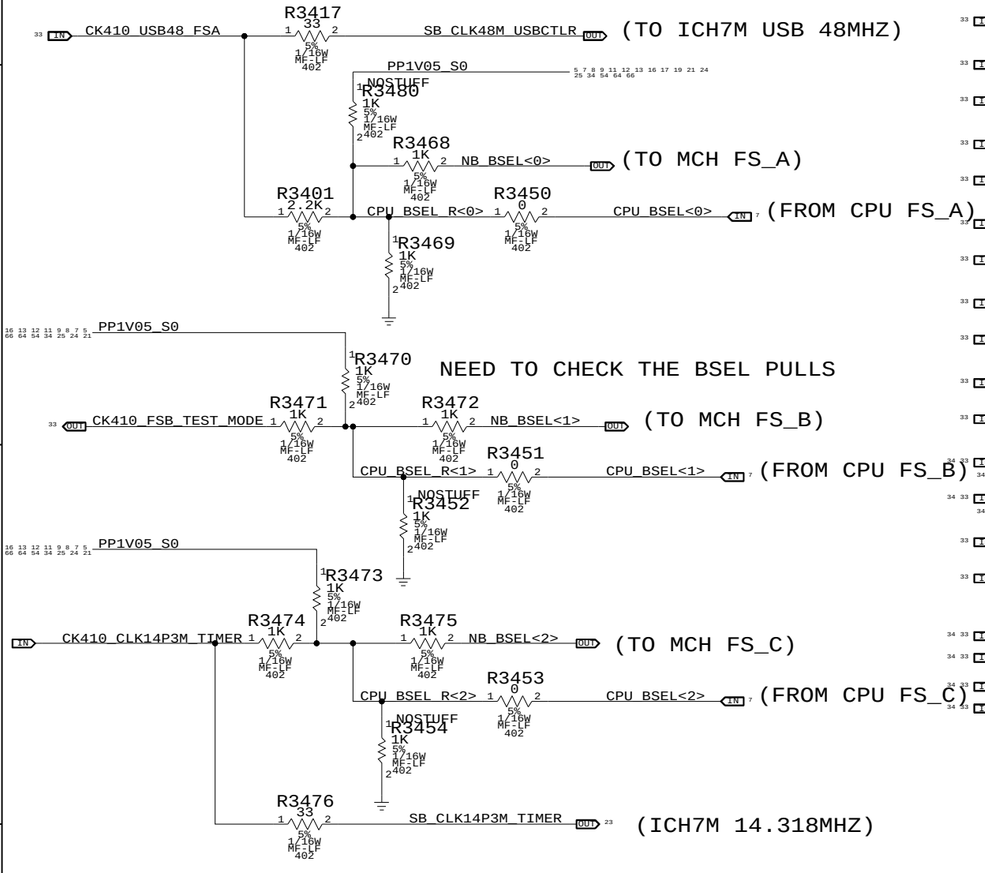

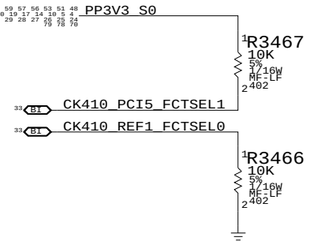

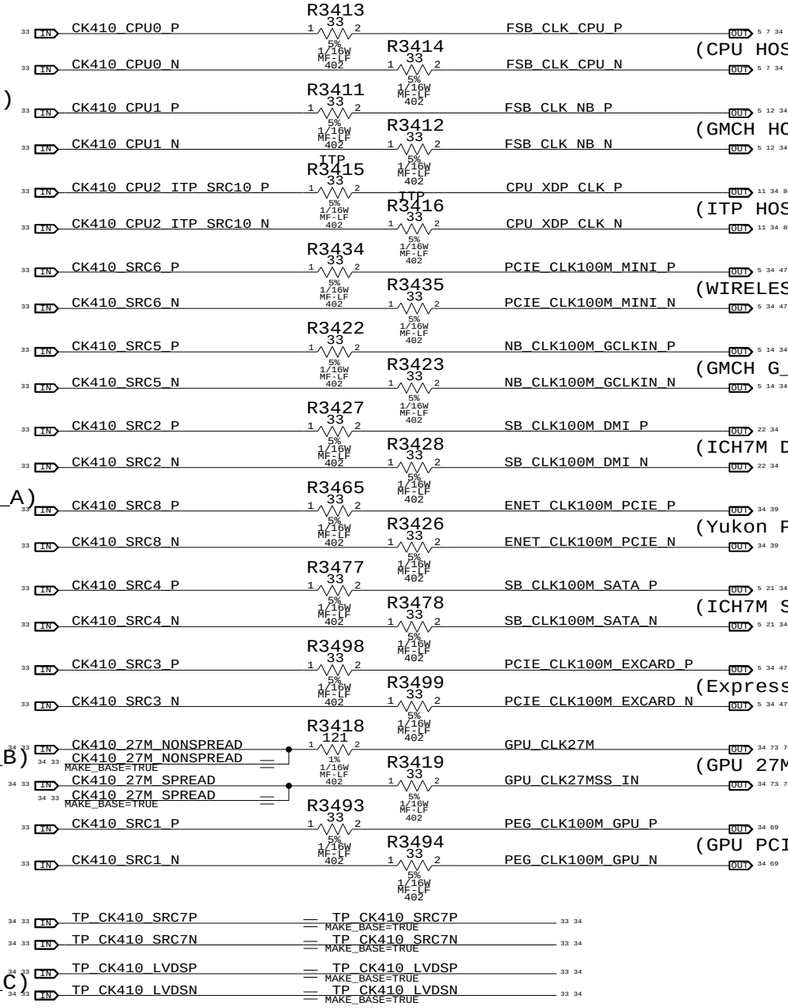

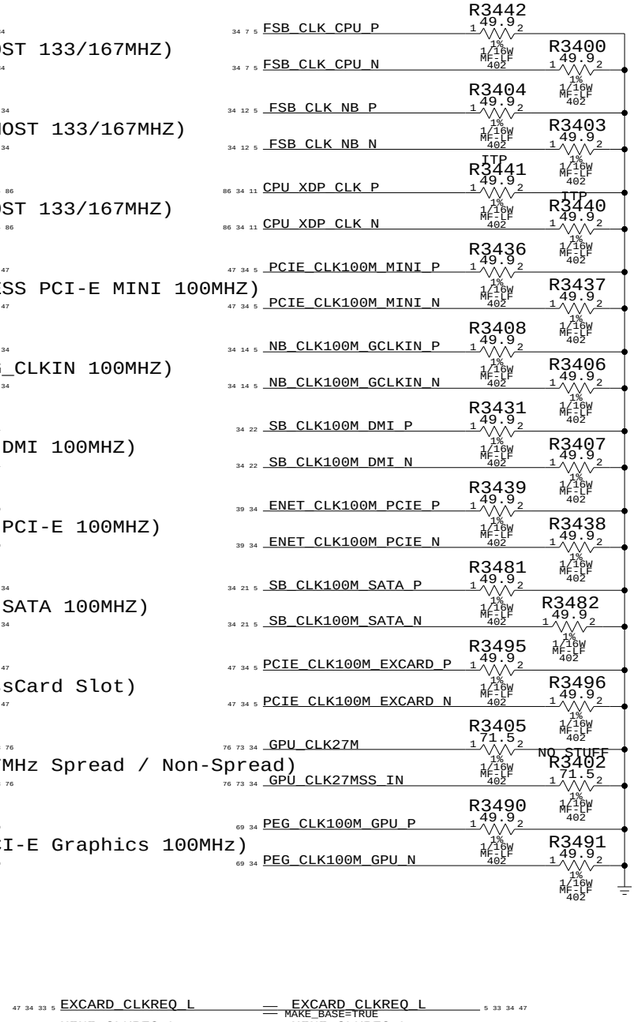

NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

Clock Termination

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE	SHT	OF
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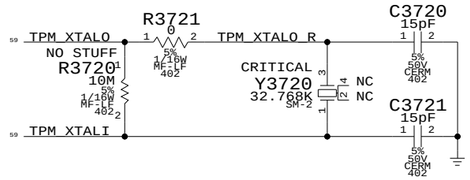
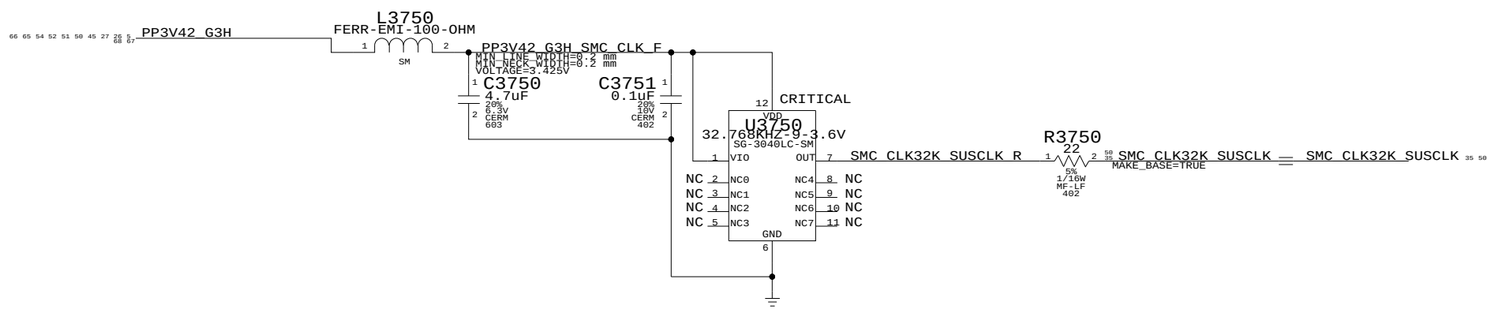
TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

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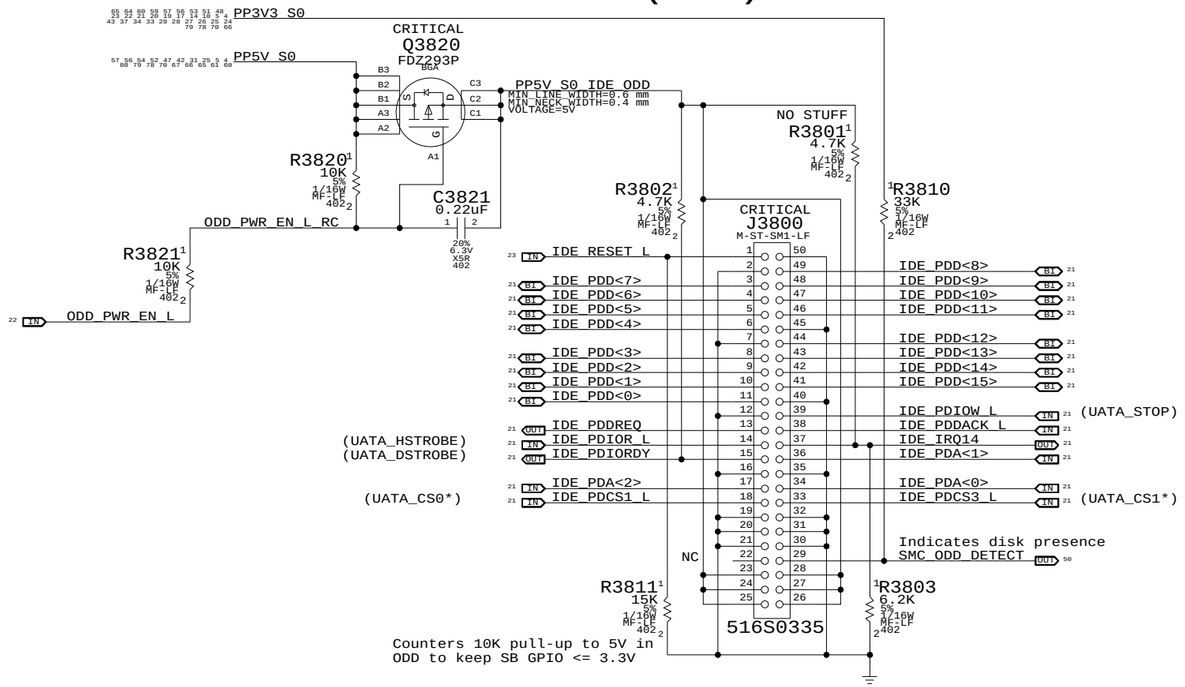
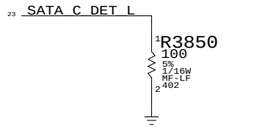
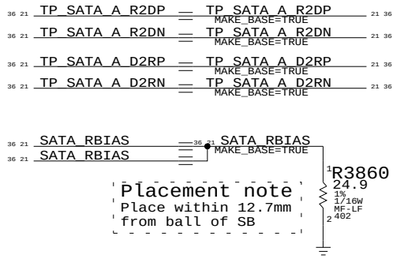
IDE (ODD) Connector







PATA Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE: NONE	SHT 36 OF 86	

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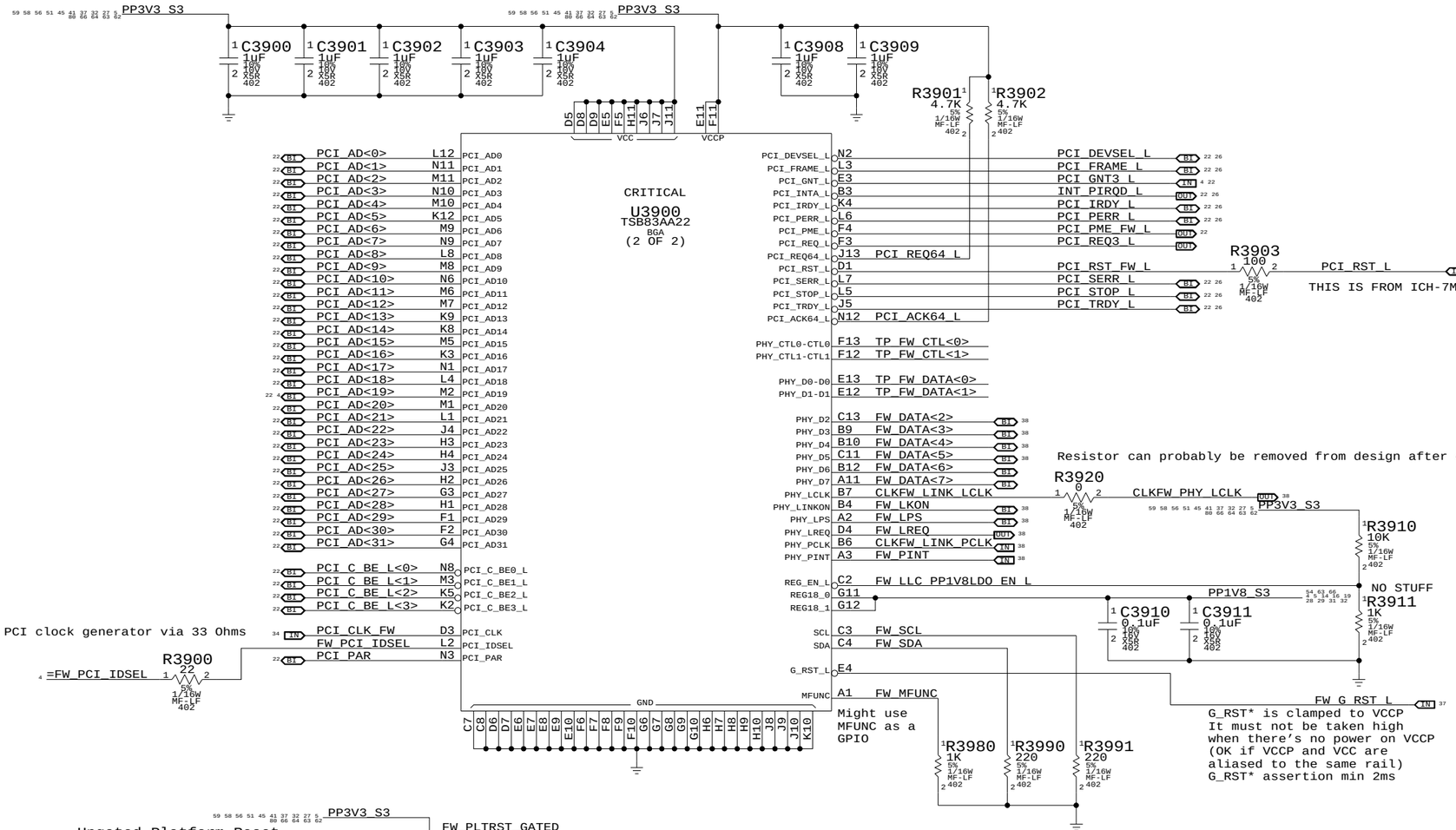

FireWire Link (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SCALE	SHT	OF
NONE	37	86

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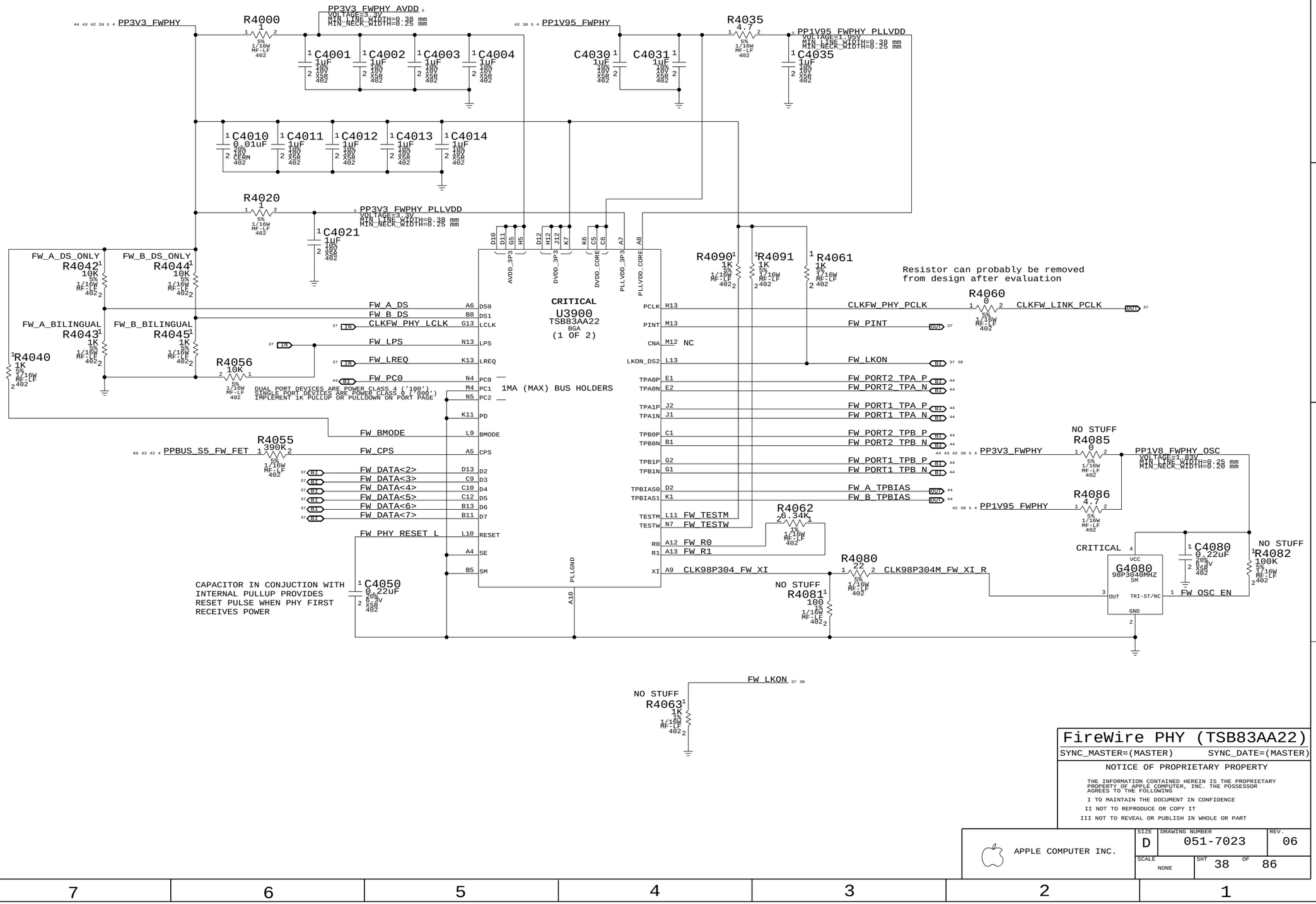

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PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01 MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402

PP2V5_S3

PLACE C4107 NEAR U4101 AVDD

PP3V3_S3AC
PP1V2_S3
PP3V3_S3AC

R4101 4.7K 5% 1/16W MF-LF 402

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF 10% 16V X5R 402

PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N
PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N

ENET_LOM_DIS_L
PM_SLP_S3_L

OMIT
CRITICAL
U4101
88E8053
QFN

OPTIONAL EXTERNAL LDO
NO PULL-UP NEEDED

ANALOG
PCI EXPRESS
MEDIA
LED
TEST
TWSI
SPI
MAIN CLK

NC_ENET_CTRL25
NC_ENET_CTRL12
ENET_RSET

R4102 4.87K 1% 1/16W MF-LF 402

ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_RST_L

C4113 0.1UF 10% 16V X5R 402

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

ENET_VPD_CLK
ENET_VPD_DATA
ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

ASF IS UNAVAILABLE ON 8053

INTERNAL PULL-UP

CRITICAL
ENET_XTALI
ENET_XTALO

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

Y4101 SM-3.2X2.5MM 25.0000M
C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

THRML_PAD

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

R4106 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402

ENET_MDI0
ENET_MDI1
ENET_MDI2
ENET_MDI3

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

PLACE RESISTORS CLOSE TO U4101

PP3V3_S3AC

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

PP3V3_S3AC

PLACE C4140 NEAR U4102 VCC

C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL
U4102
M24C08
SO8

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

ENET_VPD_DATA
ENET_VPD_CLK

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

PP1V2_S3

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

PP3V3_S3AC

C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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D	051-7023	06

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED	ENETCONN	ENET_100D	ENETCONN_P<0> 40
	ENETCONN	ENET_100D	ENETCONN_N<0> 40
BY	ENETCONN	ENET_100D	ENETCONN_P<1> 40
	ENETCONN	ENET_100D	ENETCONN_N<1> 40
ETHERNET	ENETCONN	ENET_100D	ENETCONN_P<2> 40
	ENETCONN	ENET_100D	ENETCONN_N<2> 40
PHY	ENETCONN	ENET_100D	ENETCONN_P<3> 40
	ENETCONN	ENET_100D	ENETCONN_N<3> 40

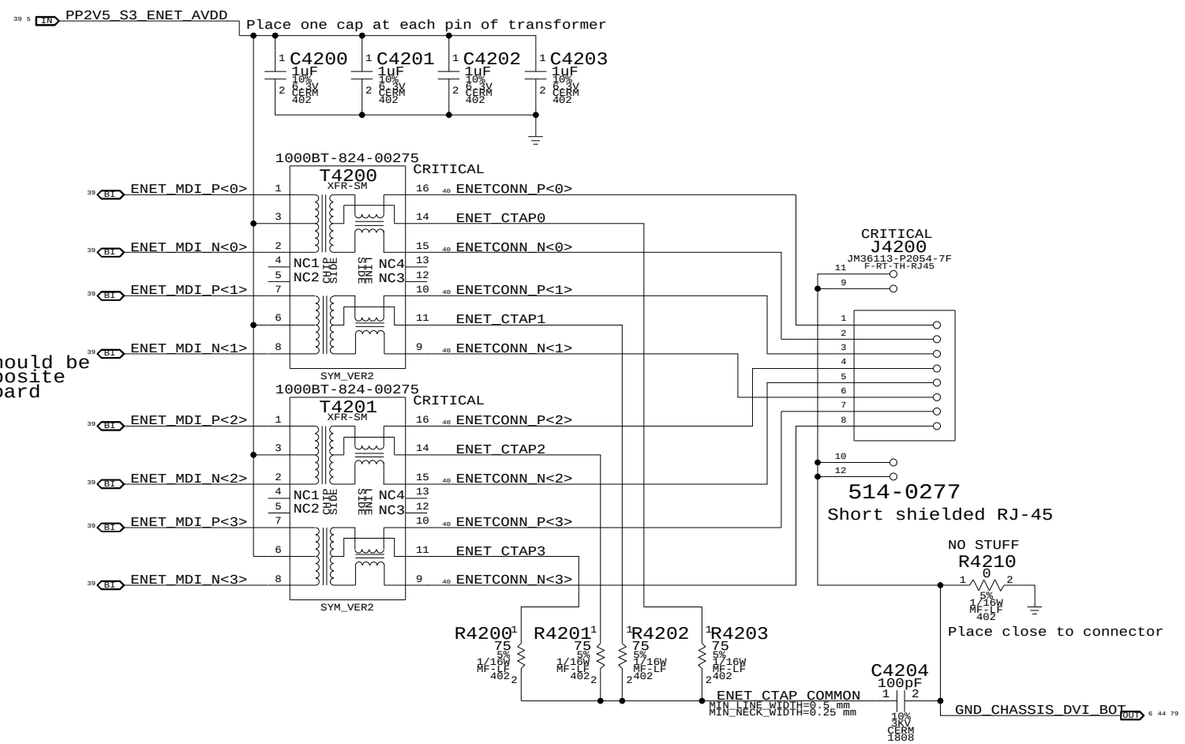
Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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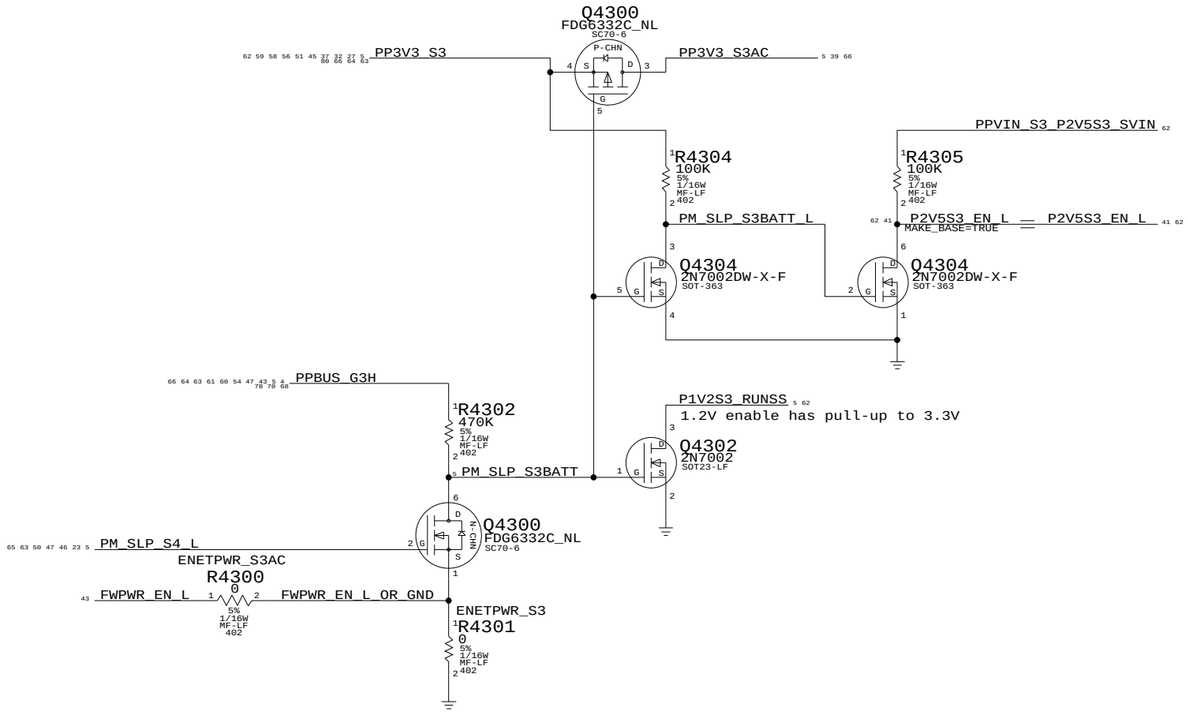
Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	3.3V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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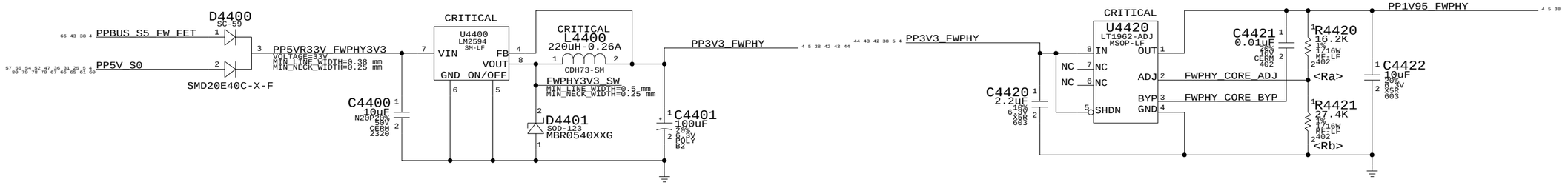
165MA MAX LOAD



Vout = 1.22V * (1 + Ra/Rb) + (Iadj * Ra)
Iadj = 30nA @ 25 deg C

FW PHY Power Supply			
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)		

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APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7023	REV: 06
	SCALE: NONE	SHT 42 OF 86	

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Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch

PPBUS_G3H

CRITICAL
F4565
1.1A-24V
MINISMDC

PPBUS_S5_FWPWRSW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

CRITICAL
Q4565
NDS9407
SOI-LF

PPBUS_S5_FW_FET_D_R
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

R4570
0.02
0.5%
1W
MF
0612

PPBUS_S5_FW_FET_D
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V

CRITICAL
D4565
SMB
B340XF

PPBUS_S5_FW_FET

R4565
470K
5%
1/16W
MF-LF
402

C4565
0.01uF
25V
16V
CERM
402

FWPWR_EN_L_DIV
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

R4566
330K
5%
1/16W
MF-LF
402

FWPWR_EN_L
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

Enables port power when machine is running or on AC.

SMC_ADAPTER_EN

Q4560
2N7002DW-X-F
SOT-363

PM_SLP_S3_L

Q4560
2N7002DW-X-F
SOT-363

PP3V3_S0

VIN+ VIN-
U4595
INA194
SOT23-5
V+ OUT
50V/V
GND

C4595
1uF
10%
16V
CERM
402

CRITICAL

FWPWR_IOUT
1A = 1V

FireWire Port Current Sense

Current Limit/Active Late-VG Protection

Late-VG Event Detection

PP2V4_FWLATEVG

PP3V3_FWPHY

R4501
10K
5%
1/16W
MF-LF
402

R4505
10K
1%
1/16W
MF-LF
402

PP2V4_FWLATEVG_RC

FWLATEGV_3V_REF

R4506
80.6K
1%
1/16W
MF-LF
402

C4501
100pF
5%
50V
CERM
402

U4500
LMC7211
SM-LF

R4500
200K
1%
1/16W
MF-LF
402

C4500
0.1UF
10%
16V
CERM
402

LATEVG_EVENT_L

D4500
SOD-123
MBR0540XXG

R4509
2.0M
5%
1/16W
MF-LF
402

FW_PORT_FAULT_PU

R4529
100K
5%
1/16W
MF-LF
402

FW_PORT_FAULT_L

FW_PORTPWR_EN

C4509
0.33uF
10%
16V
CERM-X5R
603

FWLATEVG_3V_REF:
2.95V when port power is on
2.81V when port power is off

PPBUS_S5_FW_FET

CRITICAL
R4520
0.020
1%
0.25W
MF
805

PPFW_PORTA_ISENSE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V

CRITICAL
U4520
MAX5944
SOIC

INA
ONQ1
ONA
INB
ONB
FAULTA_L
FAULTB_L
GND
SENSEA
OUTA
GATE2A
GATE1A
SENSEB
OUTB
GATE2B
GATE1B

NC

FW_PORTA_PWRCTRL

FW_PORTB_PWRCTRL

NC

C4520
1uF
10%
35V
X7R
805

C4525
1uF
10%
35V
X7R
805

CRITICAL
R4525
0.020
1%
0.25W
MF
805

PPFW_PORTB_ISENSE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V

NO STUFF
R4521
0
5%
1/4W
MF-LF
805

Q4520
SI2318DS
SOT23-3

PPFW_PORTA_VP_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V

Q4525
SI2318DS
SOT23-3

PPFW_PORTB_VP_UF
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V

NO STUFF
R4526
0
5%
1/4W
MF-LF
805

Current Limits

0.020 ohm => 2.4A
0.025 ohm => 2A
0.030 ohm => 1.66A (Ideal)
0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

FireWire Port Power

SYNC_MASTER=(M1_MLB) SYNC_DATE=(11/03/2005)

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED	FW	FW_110D	FW_PORT1_TPA_FL_P
	FW	FW_110D	FW_PORT1_TPA_FL_N
BY	FW	FW_110D	FW_PORT1_TPB_FL_P
	FW	FW_110D	FW_PORT1_TPB_FL_N
PHY	FW	FW_110D	FW_PORT2_TPA_FL_P
	FW	FW_110D	FW_PORT2_TPA_FL_N
PAGE	FW	FW_110D	FW_PORT2_TPB_FL_P
	FW	FW_110D	FW_PORT2_TPB_FL_N

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

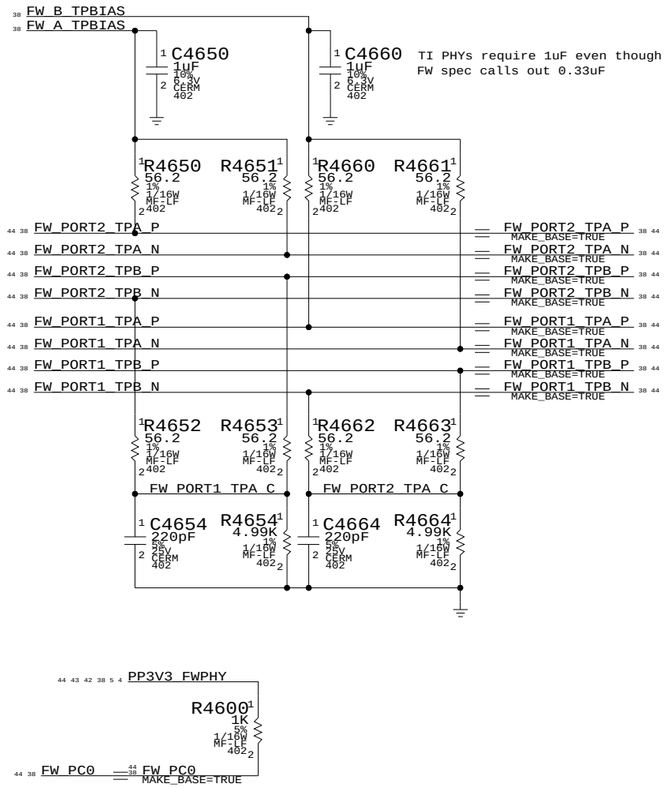
AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

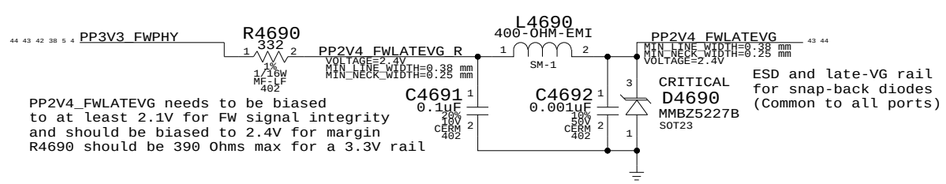
BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Termination

Place close to FireWire PHY

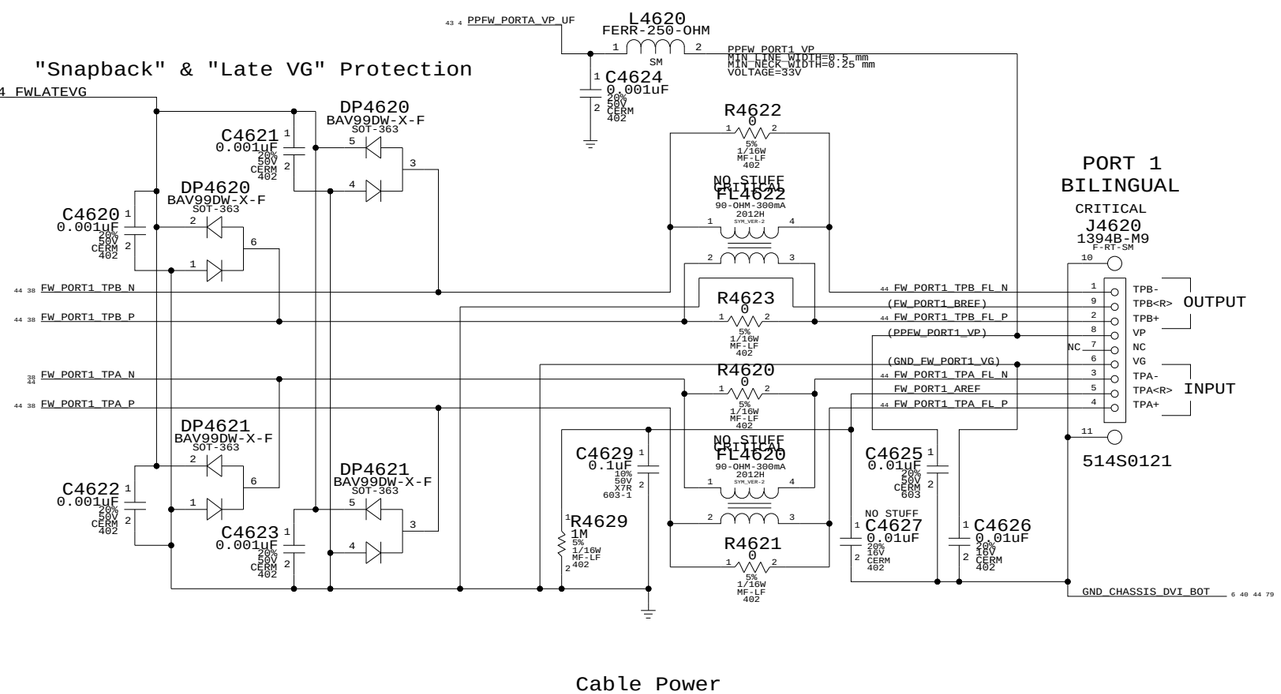


Late-VG Protection Power


PP3V3_FWPHY
R4690 332 1% 1/16W MF-LF 402
PP2V4_FWLATEVG_R
VOLTAGE=2.4V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
L4690 400-OHM-EMI SM-1
PP2V4_FWLATEVG
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.4V
C4691 0.1uF 10% 25V CERM 402
C4692 0.001uF 10% 50V CERM 402
CRITICAL
D4690 MMBZ5227B SOT23
PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4690 should be 390 Ohms max for a 3.3V rail
ESD and late-VG rail for snap-back diodes (Common to all ports)

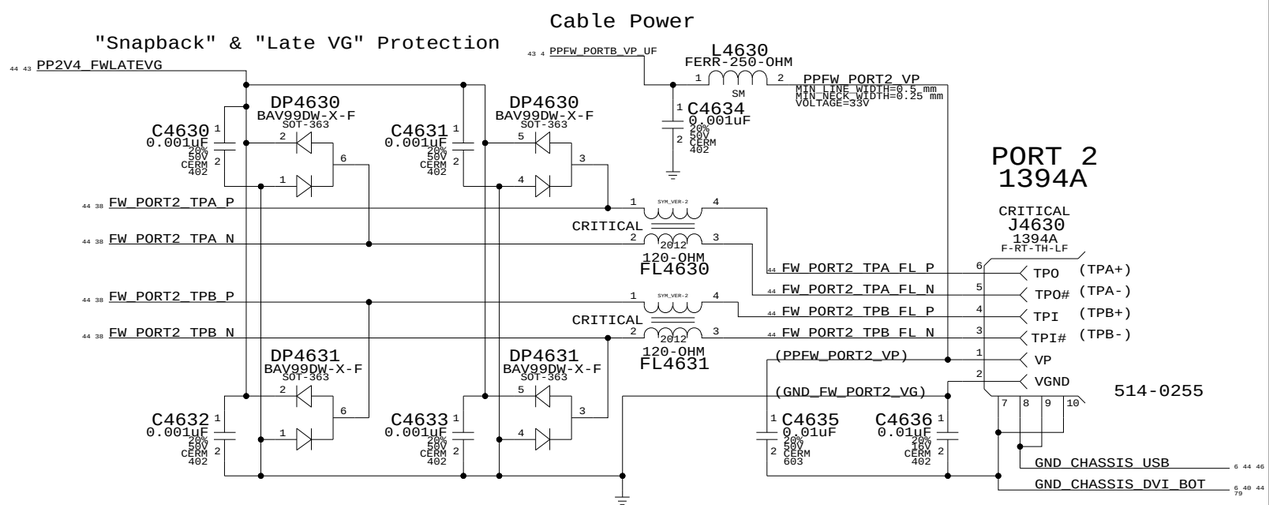
Cable Power

"Snapback" & "Late VG" Protection



Cable Power

"Snapback" & "Late VG" Protection



R4699 0 5% 1/16W MF-LF 402 — GND_CHASSIS_USB

FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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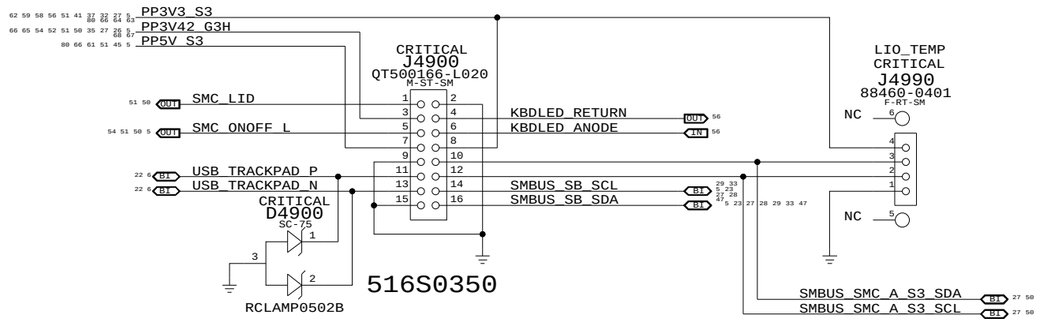
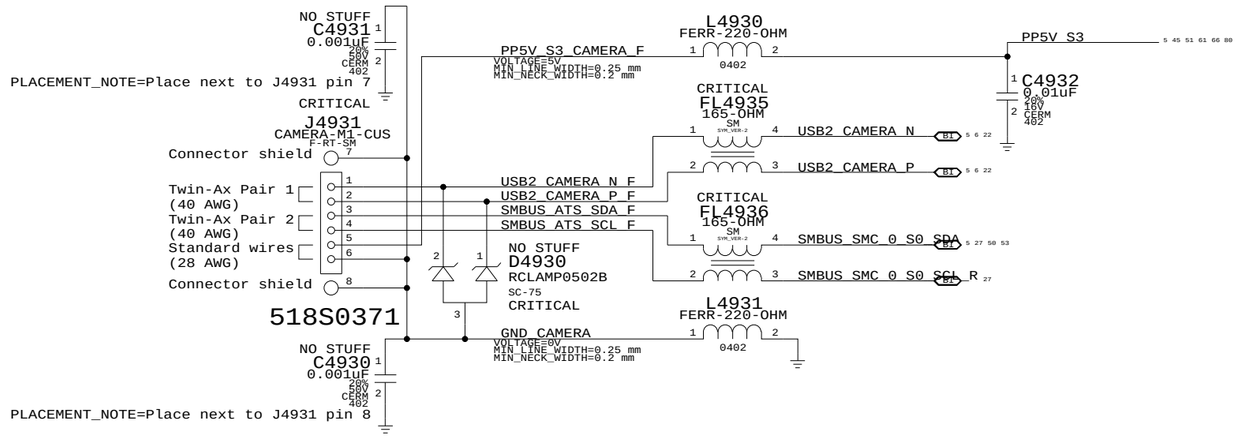
Top-Case Connector



LIO Temp Sensor Connector

Camera Connector



Internal USB Connections

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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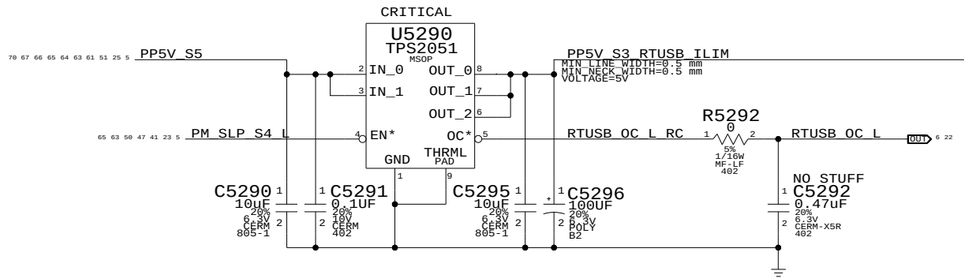
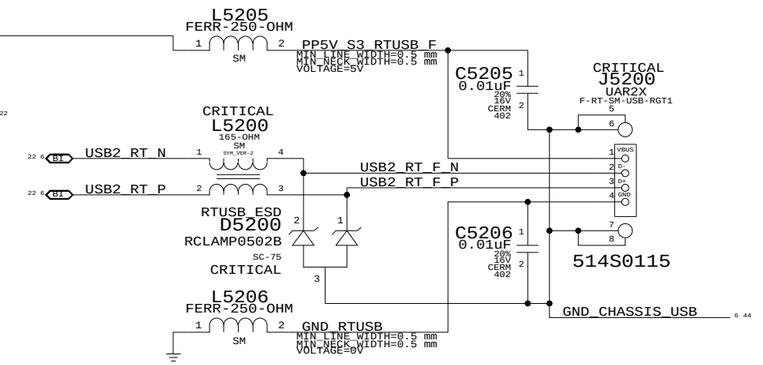
Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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D	051-7023	06

SCALE	SHT	OF
NONE	46	86

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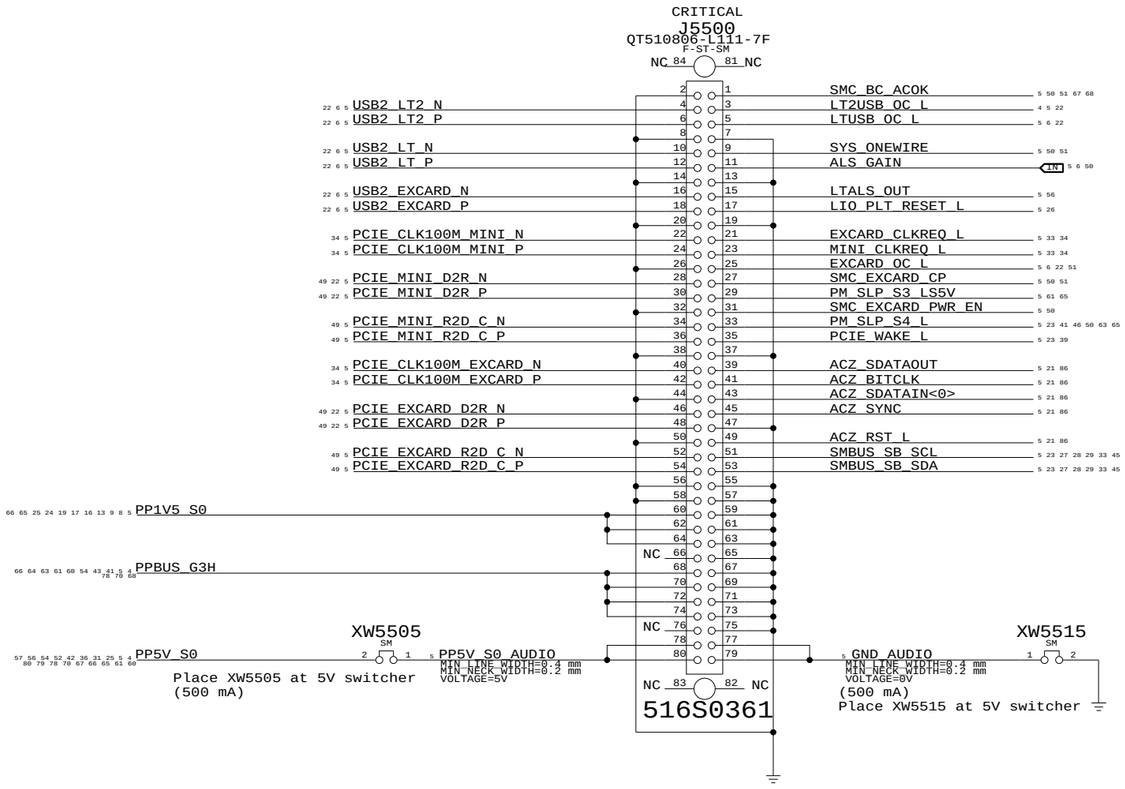
Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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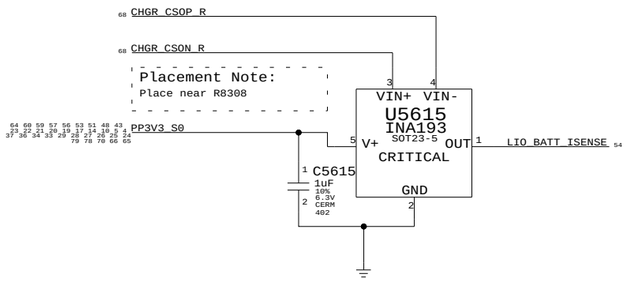
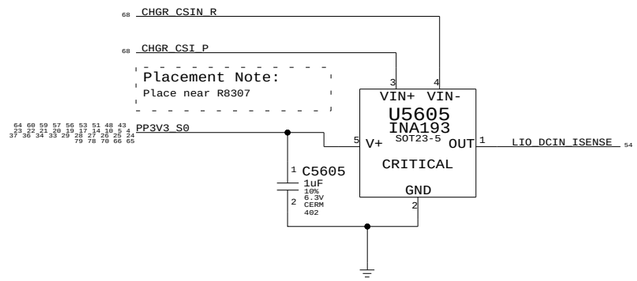
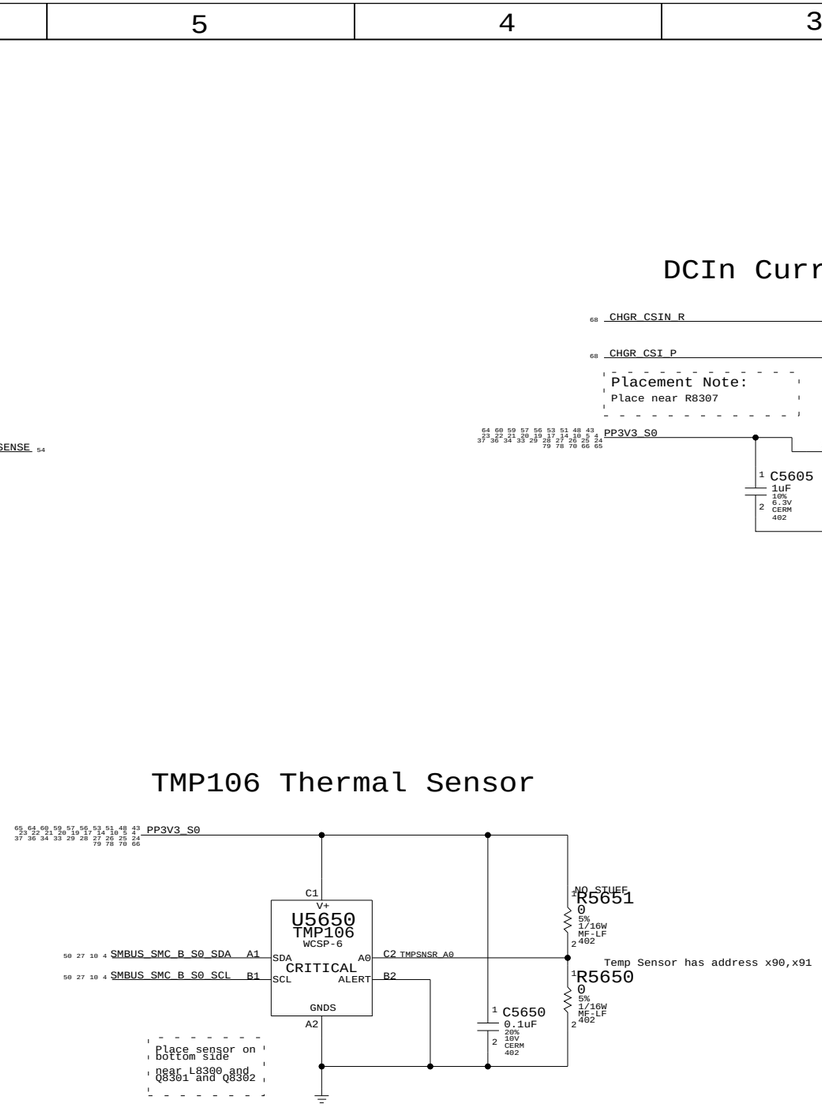
Battery Current Sense



DCIn Current Sense



TMP106 Thermal Sensor



Current & Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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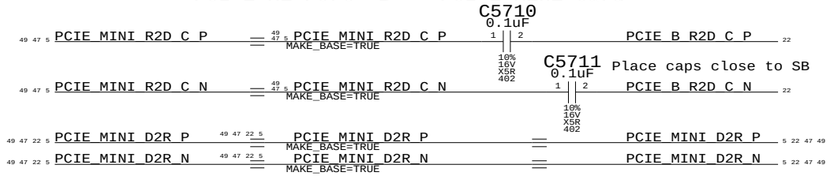
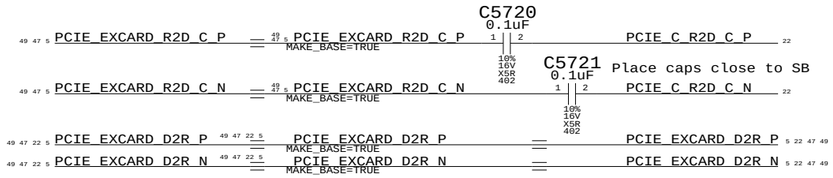
PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card



PCI-E x1 Port "C" = ExpressCard



PCI-E x1 Port "D" = Unused

TP_PCIE_D_R2DP — TP_PCIE_D_R2DP
TP_PCIE_D_R2DN — TP_PCIE_D_R2DN
TP_PCIE_D_D2RP — TP_PCIE_D_D2RP
TP_PCIE_D_D2RN — TP_PCIE_D_D2RN
MAKE_BASE=TRUE

PCI-E x1 Port "E" = Unused

TP_PCIE_E_R2DP — TP_PCIE_E_R2DP
TP_PCIE_E_R2DN — TP_PCIE_E_R2DN
TP_PCIE_E_D2RP — TP_PCIE_E_D2RP
TP_PCIE_E_D2RN — TP_PCIE_E_D2RN
MAKE_BASE=TRUE

PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP — TP_PCIE_F_R2DP
TP_PCIE_F_R2DN — TP_PCIE_F_R2DN
TP_PCIE_F_D2RP — TP_PCIE_F_D2RP
TP_PCIE_F_D2RN — TP_PCIE_F_D2RN
MAKE_BASE=TRUE

PCI-E Connections

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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D	051-7023	06

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UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
(1 OF 4)

PM_LAN_ENABLE	B12	P10	
SMC_RSTGATE_L	C13	P11	
ALL_SYS_PWRGD	A15	P12	
RSMRST_PWRGD	B14	P13	
SMC_SB_NMI	B15	P14	
PM_RSMRST_L	C14	P15	
IMVP_VR_ON	D12	P16	
PM_PWRBTN_L	C15	P17	
TP_SMC_P20	D13	P20	
TP_SMC_P21	D14	P21	
TP_SMC_P22	D15	P22	
TP_SMC_P23	E12	P23	
SMC_BATT_TRICKLE_EN	E14	P24	
SMC_BATT_CHG_EN	E15	P25	
TP_SMC_P26	E13	P26	
TP_SMC_P27	F14	P27	
LPC_AD<0>	D9	P30/LAD0	
LPC_AD<1>	C9	P31/LAD1	
LPC_AD<2>	A9	P32/LAD2	
LPC_AD<3>	B9	P33/LAD3	
LPC_FRAME_L	D8	P34/LFRAME*	
SMC_LRESET_L	C8	P35/LRESET*	
PCI_CLK_SMC	A8	P36/LCLK	
INT_SERIRQ	D7	P37/SERIRQ	
TP_SMC_XDP_TMS	A5	P40/TMI0	
SMC_SYS_LED_16B	B5	P41/TMO0	
SMBUS_SMC_BSB_SDA	D5	P42/SDA1	
SMC_TPM_PP	C3	P43/TMI1/EXSCKL	
TP_SMC_XDP_TRST_L	B1	P44/TMO1	
TP_SMC_XDP_TCK	C2	P45	
TP_SMC_SYS_LED	D3	P46/PWX0/PWM0	
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1	
SMC_TX_L	G1	P50	
SMC_RX_L	G4	P51	
SMBUS_SMC_0_S0_SCL	F2	P52/SCL0	

P60/KIN0*	L13	SMC_PM_G2_EN	
P61/KIN1*	L14	SMC_ADAPTER_EN	
P62/KIN2*	L15	SPI_ARB	
P63/KIN3*	K12	SPI_SCLK	
P64/KIN4*	K13	SPI_SI	
P65/KIN5*	K14	SPI_SO	
P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3	
P67/IRQ7*/KIN7*	J13	FWH_INIT_L	
P70/AN0	N12	SMC_CPU_ISENSE	
P71/AN1	R13	SMC_CPU_VSENSE	
P72/AN2	P13	SMC_GPU_ISENSE	
P73/AN3	R14	SMC_GPU_VSENSE	
P74/AN4	P14	SMC_DCIN_ISENSE	
P75/AN5	R15	SMC_PBUS_VSENSE	
P76/AN6	N13	SMC_BATT_ISENSE	
P77/AN7	P15	SMC_FWIRE_ISENSE	
P80/PME*	C7	SMC_WAKE_SCI_L	
P81/GA20	A7	SMC_TPM_GPIO	
P82/CLKRUN*	B7	PM_CLKRUN_L	
P83/LPCPD*	D6	PM_SUS_STAT_L	
P84/IRQ3*/TXD1	C6	SC_TX_L	
P85/IRQ4*/RXD1	A6	SC_RX_L	
P86/IRQ5*/SCK1/SCL1	B6	SMBUS_SMC_BSB_SCL	
P90/IRQ2*	K4	SMC_ONOFF_L	
P91/IRQ1*	J2	SMC_BC_ACOK	
P92/IRQ0*	J1	SMC_BS_ALRT_L	
P93/IRQ12*	J3	PM_SLP_S3_L	
P94/IRQ13*	J4	PM_SLP_S4_L	
P95/IRQ14*	H2	PM_SLP_S5_L	
P96/EXCL	H1	SMC_CLK32K_SUSCLK	
P97/IRQ15*/SDA0	G2	SMBUS_SMC_0_S0_SDA	

OMIT
U5800
SMC_H8S2116
BGA
(2 OF 4)

SMC_RCIN_L	R3	PA0/KIN8*/PA2PC	
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	
SMC_TPM_RESET_L	N3	PA3/KIN11*/PS2AD	
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	
PM_THRM_L	N2	PA5/KIN13*/PS2BD	
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	
SMC_EXTSMI_L	B10	PB0/LSMI*	
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	
SMC_ODD_DETECT	D10	PB2	
ISENSE_CAL_EN	A11	PB3	
SMC_EXCARD_CP	B11	PB4	
SMC_EXCARD_PWR_EN	C11	PB5	
SMC_EXCARD_OC_L	A12	PB6	
SMC_XDP_TDO_3_3	D11	PB7	
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	
TP_SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	
TP_SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	
TP_SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	
TP_SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	
SMS_X_AXIS	M11	PD0/AN8	
SMS_Y_AXIS	P11	PD1/AN9	
SMS_Z_AXIS	R11	PD2/AN10	
TP_SMC_ANALOG_ID	N11	PD3/AN11	
SMC_P1V05S0_ISENSE	P10	PD4/AN12	
SMC_P1V8S3_ISENSE	R10	PD5/AN13	
ALS_LEFT	N10	PD6/AN14	
ALS_RIGHT	M10	PD7/AN15	

PE0	M3	SMC_CASE_OPEN	
PE1*/ETCK	M2	SMC_TCK	
PE2*/ETDI	M1	SMC_TDI	
PE3*/ETDO	L4	SMC_TDO	
PE4*/ETMS	L2	SMC_TMS	
PF0/IRQ8*/PWM2	M7	TP_SMC_PF0	
PF1/IRQ9*/PWM3	P6	TP_SMC_PF1	
PF2/IRQ10*/TMOY	R6	SMC_LID	
PF3/IRQ11*/TMOX	N6	SMC_CPU_RESET_3_3_L	
PF4/PWM4	M6	SMC_BATT_ISET	
PF5/PWM5	R5	TP_SMC_BATT_VSET	
PF6/PWM6	P5	SMC_SYS_ISET	
PF7/PWM7	N5	TP_SMC_SYS_VSET	
PG0/EXIRQ8*/TMIX	P9	SPI_CE_L	
PG1/EXIRQ9*/TMIY	R9	SMC_XDP_TCK_3_3	
PG2/EXIRQ10*/SDA2	N9	SMBUS_SMC_BSA_SDA	
PG3/EXIRQ11*/SCL2	P8	SMBUS_SMC_BSA_SCL	
PG4/EXIRQ12*/EXSDAA	R8	SMBUS_SMC_A_S3_SDA	
PG5/EXIRQ13*/EXSCLA	M8	SMBUS_SMC_A_S3_SCL	
PG6/EXIRQ14*/EXSDAB	P7	SMBUS_SMC_B_S0_SDA	
PG7/EXIRQ15*/EXSCLB	R7	SMBUS_SMC_B_S0_SCL	
PH0/EXIRQ6*	E1	SMC_PROCHOT	
PH1/EXIRQ7*	F3	SMC_THRMTRIP	
PH2/FWE	K2	SMC_FWE	
PH3/EXEXCL	C4	ALS_GAIN	
PH4	D4	SMS_INT_L	
PH5	B3	SMS_ONOFF_L	

OMIT
U5800
SMC_H8S2116
BGA
(4 OF 4)

G3	NC0	NC12	E15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

PP3V42_G3H
C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 20% 6.3V CERM-X5R 402

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

VCL IS INTERNAL RAIL

PP3V42_G3H
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
C5820 0.1UF 20% 10V CERM 402
GND_SMC_AVSS

PP3V3_AVREF_SMC
PP3V42_G3H
R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

SMC_RST_L	E3	RES*	
SMC_XTAL	A2	XTAL	
SMC_EXTAL	B2	EXTAL	
MD1	E2		SMC_MD1
MD2	K1		KBC_MDE
NMI	F4		SMC_NMI
ETRST*	L1		SMC_TRST_L
AVSS	P12		
AVSS	R12		
VSS	D1		
VSS	P4		
VSS	R4		
VSS	F12		
VSS	F13		
VSS	B13		
VSS	A13		
VSS	A4		
VSS	B4		
VSS	D2		

R5898 10K 5% 1/16W MF-LF 402
R5803 10K 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402
NOSTUFF

XW5800
SM
GND_SMC_AVSS

SMC

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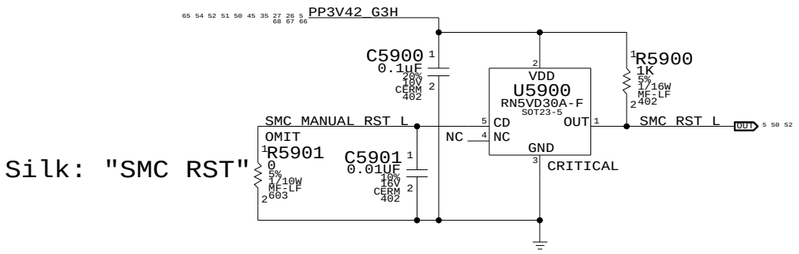
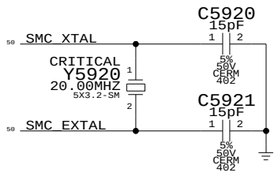
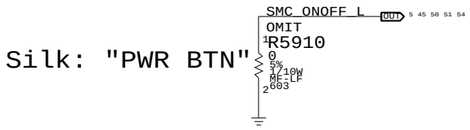
SMC Reset Button / Brownout Detect



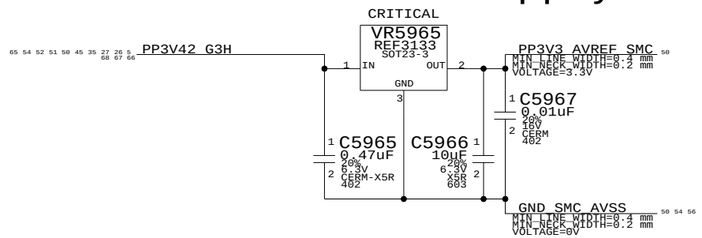
SMC Crystal Circuit



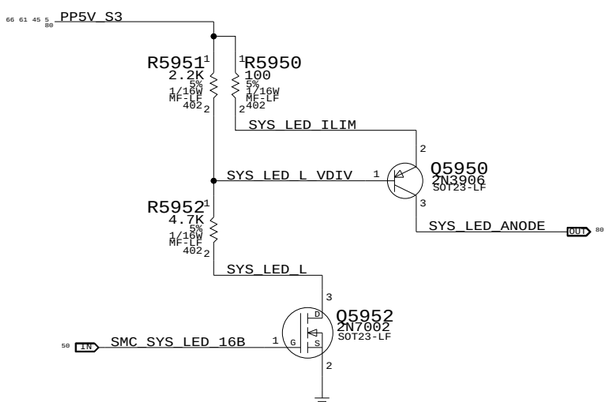
Debug Power Button



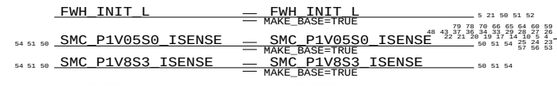
SMC AVREF Supply



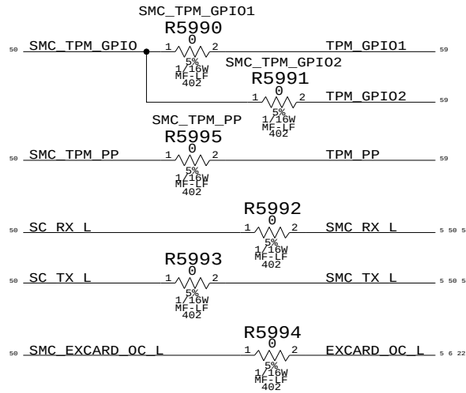
System (Sleep) LED Circuit



FWH_INIT_L

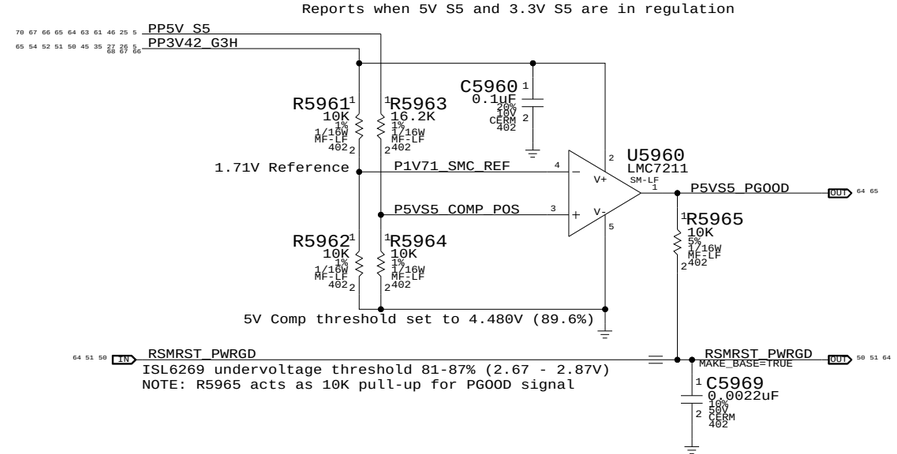


SMC_TPM_GPIO1

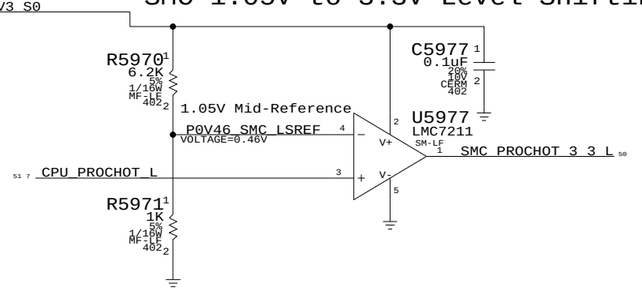


SMC PWRGD Circuit

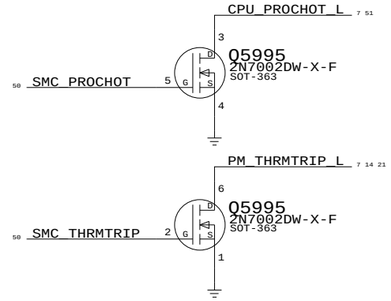
Reports when 5V S5 and 3.3V S5 are in regulation

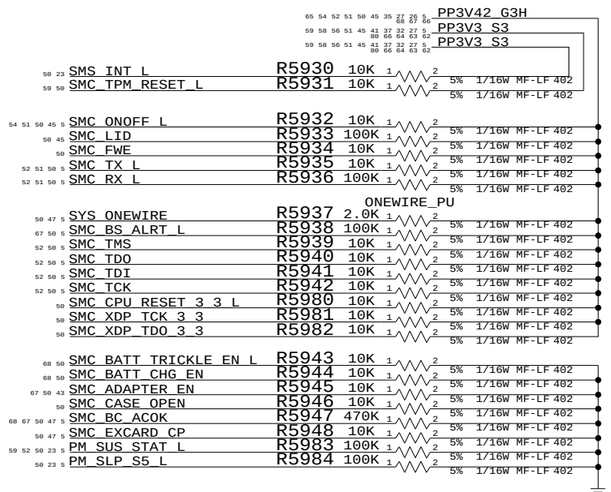

PP5V_S5
PP3V42_G3H
R5961 10K 1% 1/16W MF-LF 402
R5963 16.2K 1% 1/16W MF-LF 402
C5960 0.1uF 20% 16V CERM 402
1.71V Reference
P1V71_SMC_REF
U5960 LMC7211 SM-LF
P5VS5_PGOOD
P5VS5_COMP_POS
R5962 10K 1% 1/16W MF-LF 402
R5964 10K 1% 1/16W MF-LF 402
R5965 10K 5% 1/16W MF-LF 402
5V Comp threshold set to 4.480V (89.6%)
RSMRST_PWRGD
ISL6269 undervoltage threshold 81-87% (2.67 - 2.87V)
NOTE: R5965 acts as 10K pull-up for PGOOD signal
C5969 0.0022uF 10% 50V CERM 402

SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting





SMC Support

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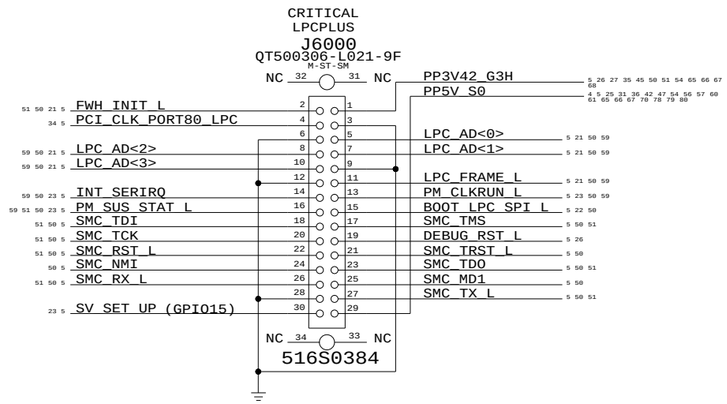

LPC+ Debug Connector

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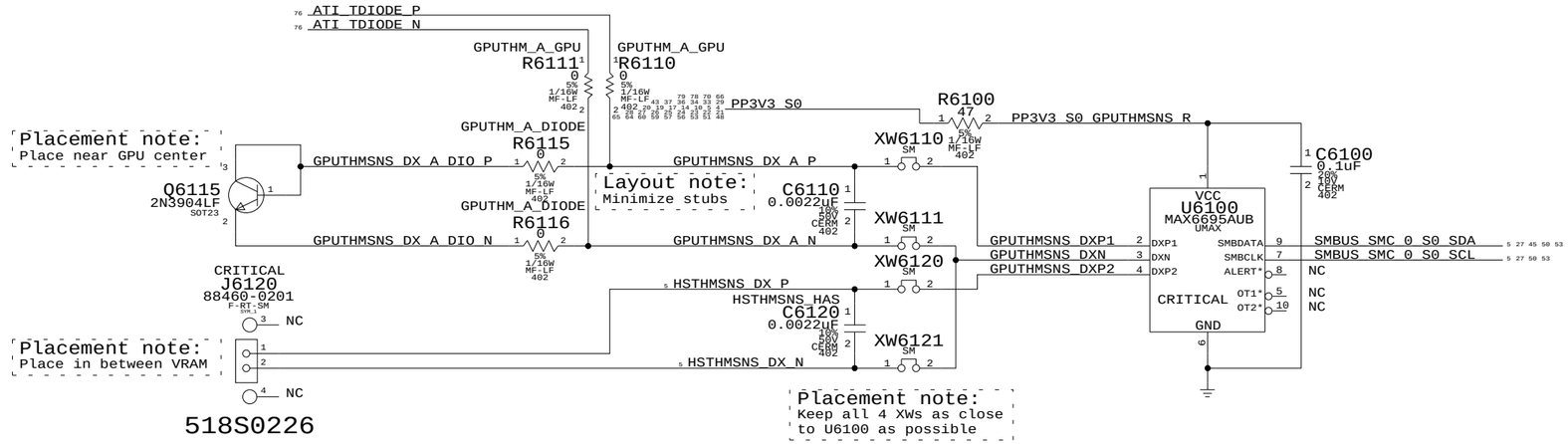
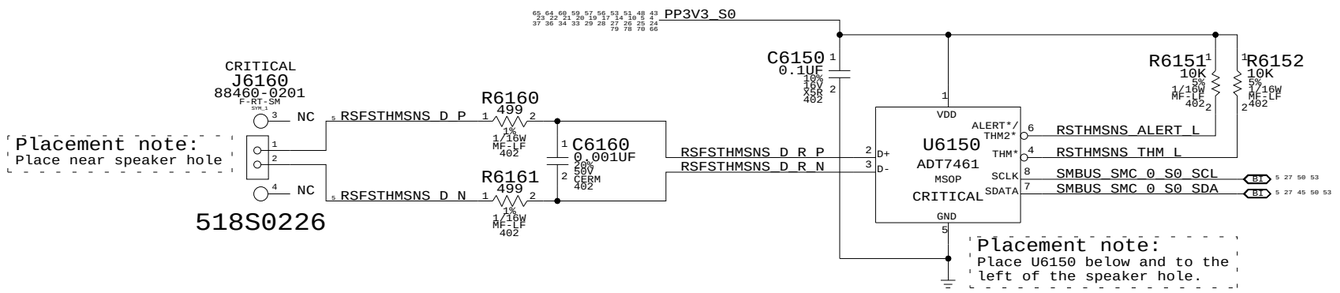
GPU / Heat Pipe Thermal Sensor

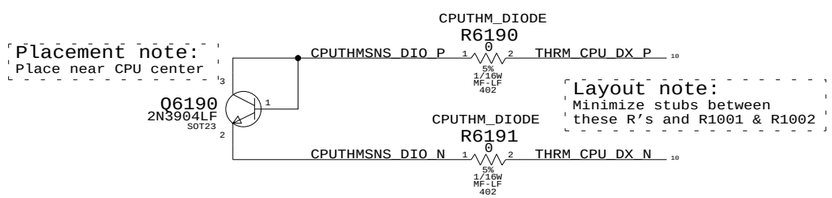


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

Thermal Sensors

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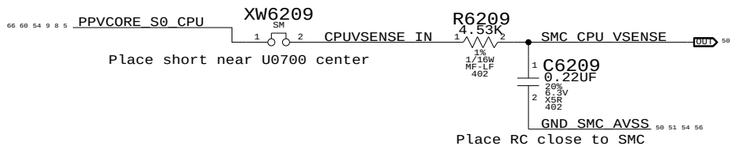
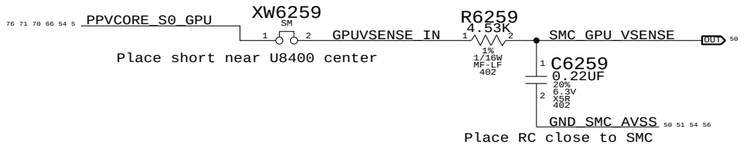
CPU Voltage Sense / Filter



Place short near U0700 center

Place RC close to SMC

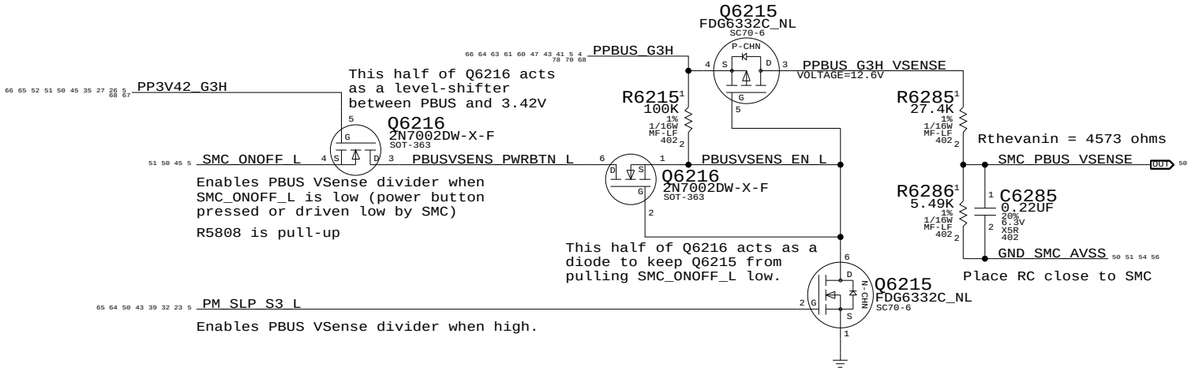
GPU Voltage Sense / Filter



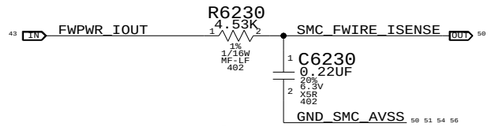
Place short near U8400 center

Place RC close to SMC

PBUS Voltage Sense Enable & Filter

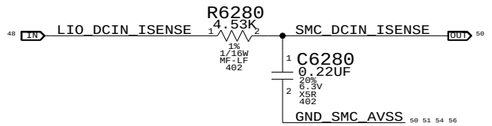


FireWire Current Sense Filter



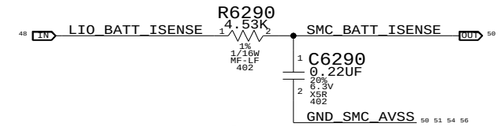
Place RC close to SMC

DCIN Current Sense Filter



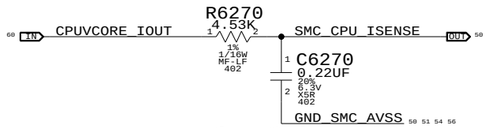
Place RC close to SMC

Battery Current Sense Filter



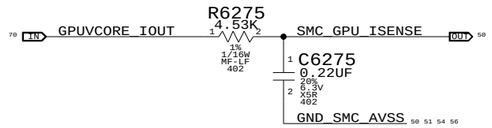
Place RC close to SMC

CPU Current Sense Filter



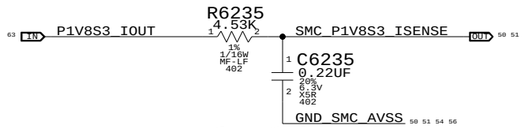
Place RC close to SMC

GPU Current Sense Filter



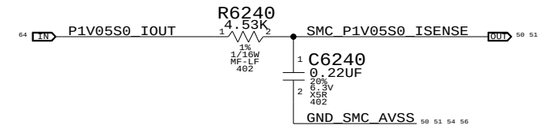
Place RC close to SMC

1.8V S3 (Memory) Current Sense Filter



Place RC close to SMC

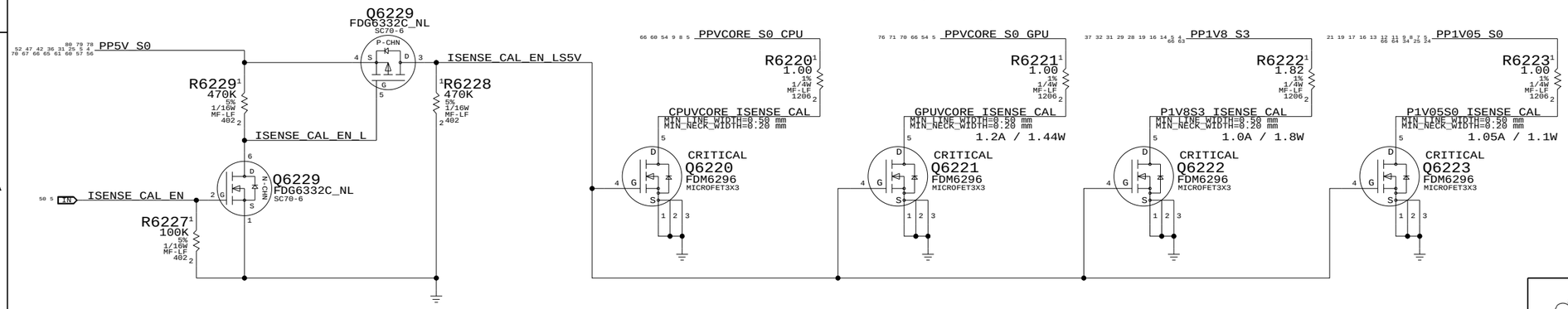
1.05V S0 (NB) Current Sense Filter



Place RC close to SMC

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing		
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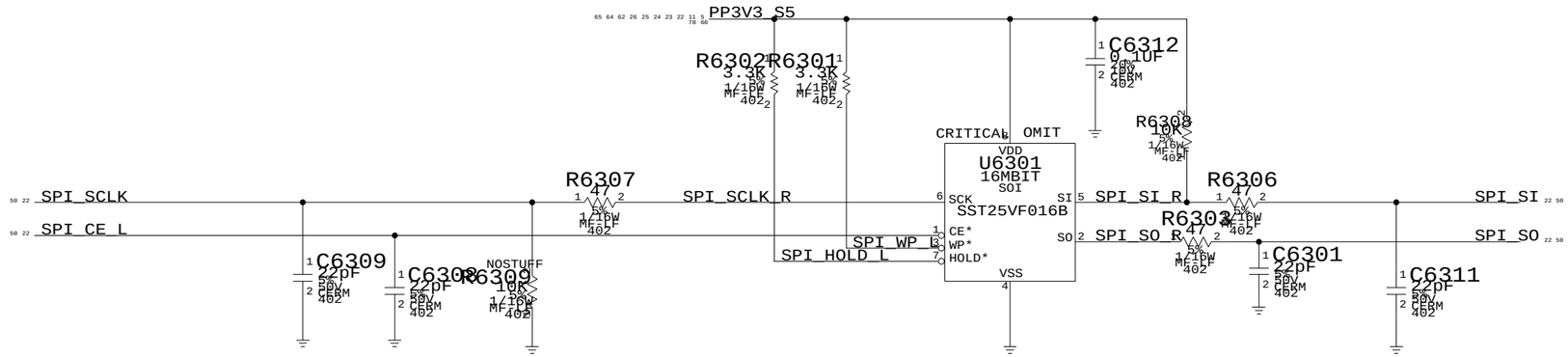

R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

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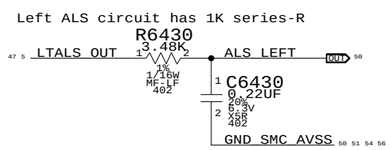
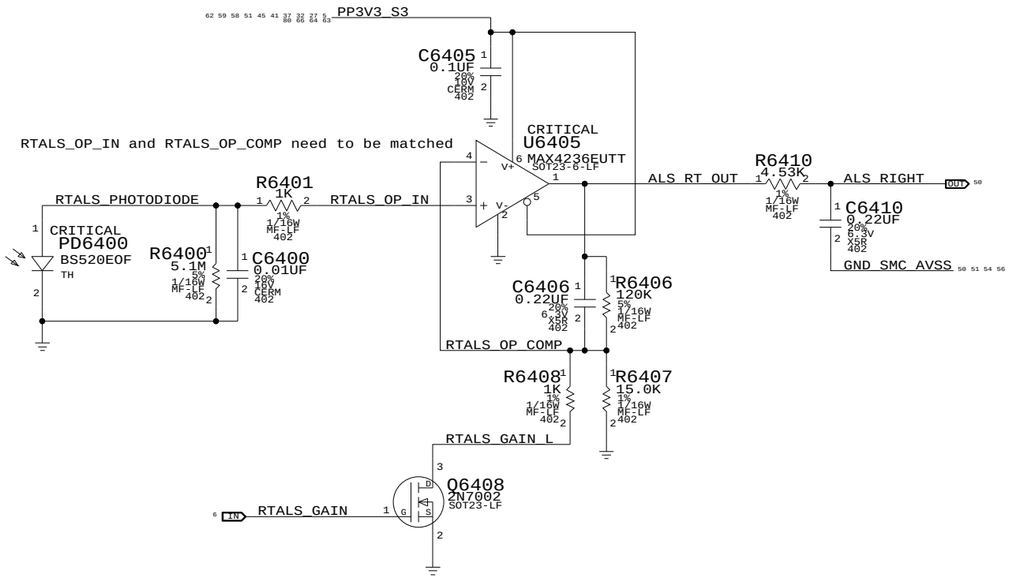
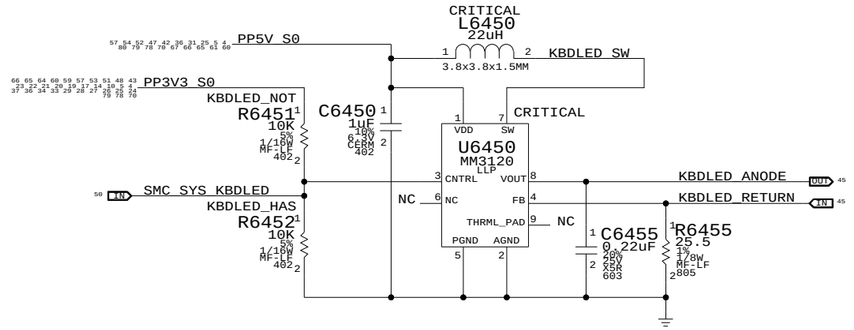
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support

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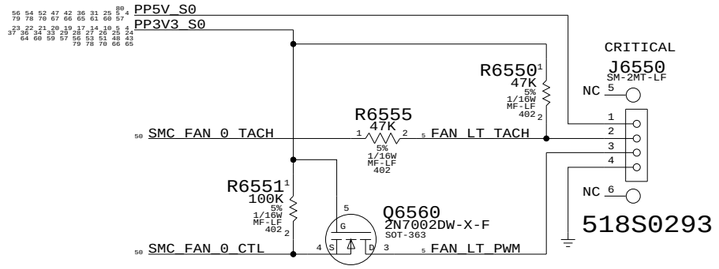
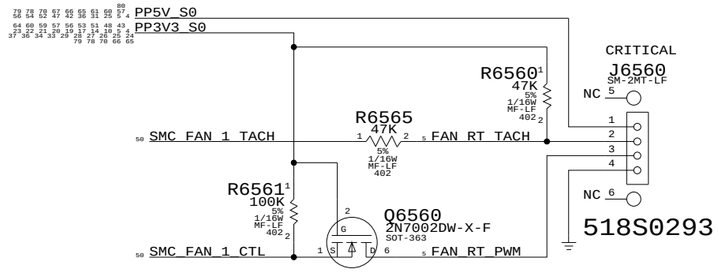
Left Fan



Right Fan



Fan Connectors

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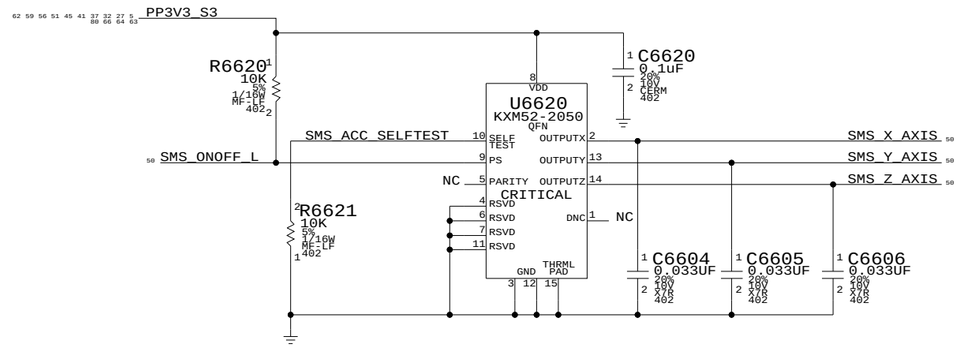
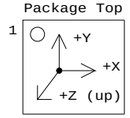


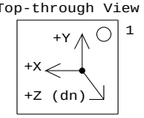
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M1 placement: Bottom-side

Sudden Motion Sensor (SMS)

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SCALE: NONE

SHT 58 OF 86

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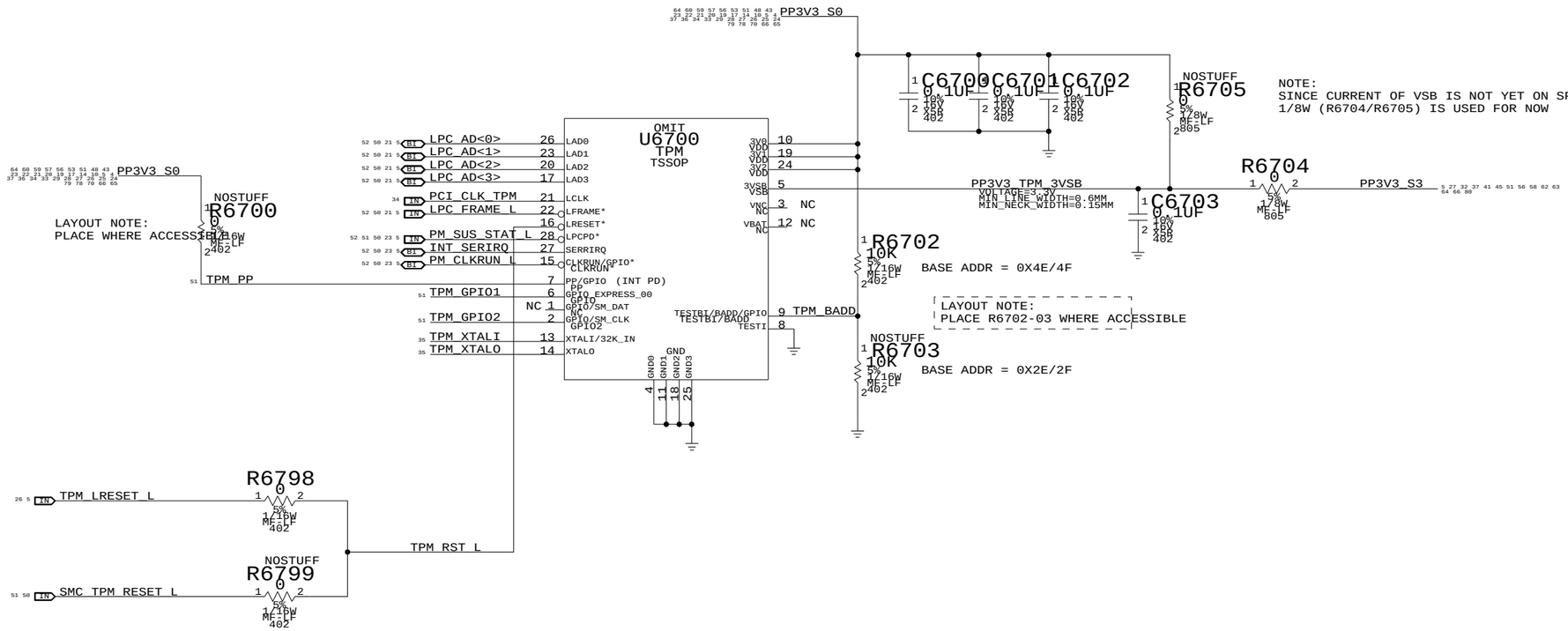

TPM

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DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

These caps for Q7500

These caps for Q7550

PPVCORE_S0_CPU
Vout = Variable
36A max output
(Inductors limit)

OMIT
U7530
ISL6262
QFN

CPU VCore Current Sense

Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

IMVP6 CPU VCore Regulator

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PPBUS_G3H

CRITICAL C7640 33uF 20% 16V POLY CASED2E-SM
C7641 1uF 10% 16V X5R 603
R7600 10 5% 1/16W MF-LF 402
CRITICAL C7680 33uF 20% 16V POLY CASED2E-SM
C7681 1uF 10% 16V X5R 603

R7623 2.26K 1% 1/16W MF-LF 402
C7623 0.1uF 10% 16V X5R 402
C7620 0.1uF 10% 16V X5R 402
R7620 3.65K 1% 1/16W MF-LF 402
R7629 6.04K 1% 1/16W MF-LF 402

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

PP5V_S5_P5VP1V5_INTVCC
CRITICAL D7624 SOD-323 CMDSH-3
P5VS5_BOOST_RC
R7624 0 5% 1/16W MF-LF 402

CRITICAL Q7620 FDM6296 MICROFET3X3
CRITICAL L7620 1.8uH-10.4A SM
C7624 0.1uF 20% 10V CERM 402
CRITICAL Q7621 FDM6296 MICROFET3X3
CRITICAL D7621 B240-X-F SMB
NO STUFF C7621 1000pF 10% 25V X7R 402

PP5V_S5_REG
Vout = 4.98V
8A max output
(L7620 limit)

CRITICAL C7652 150uF 20% 6.3V POLY SMC-LF
C7650 22UF 20% 6.3V CERM 805
C7651 22UF 20% 6.3V CERM 805

<Ra>
R7627 52.3K 1% 1/16W MF-LF 402
C7627 470pF 10% 50V CERM 402

<Rb>
R7628 10K 1% 1/16W MF-LF 402
NO STUFF C7628 1000pF 10% 25V X7R 402

GND_P5VP1V5_SGND
VOLTAGE=0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Connect to RUNSS pins to control outputs.
If unconnected, powers up with VIN.
NOTE: Be aware of pull-ups to VIN on these signals.

PPVIN_S5_P5VP1V5_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12V
C7600 1uF 10% 16V X5R 603
R7630 1M 5% 1/16W MF-LF 402
R7670 1M 5% 1/16W MF-LF 402

VIN
CRITICAL U7600 LTC3728LXC QFN

TG1	26	P5VS5_TG	
BOOST1	25	P5VS5_BOOST	
SW1	24	P5VS5_SW	
BG1	23	P5VS5_BG	
PLLIN		NC	
SENSE1+	30	P5VS5_SNS_P	
SENSE1-		P5VS5_SNS_N	
VOSENSE1	1	P5VS5_VOSNS	
ITH1	5	P5VS5_ITH	
RUN_SS1	28	P5VS5_RUNSS	
FCB	4		
EXTVCC	21		
TG2	14	P1V5S0_TG	
BOOST2	17	P1V5S0_BOOST	
SW2	15	P1V5S0_SW	
BG2	18	P1V5S0_BG	
PLLFLTR	2	P5VP1V5_FSEL	
SENSE2+	12	P1V5S0_SNS_R_P	
SENSE2-	11	P1V5S0_SNS_R_N	
VOSENSE2	9	P1V5S0_VOSNS	
ITH2	8	P1V5S0_ITH	
RUN_SS2	13	P1V5S0_RUNSS	
3_3VOUT	7	NC	
PGOOD	27		
INTVCC	20		
NC1	10	NC	
NC2	16	NC	
NC3	29	NC	
NC4	32	NC	
SGND	6		
THRML_PAD	33		
PGND	19		

C7622 0.001uF 10% 16V CERM 402
C7626 47pF 5% 50V CERM 402
C7625 470pF 10% 50V CERM 402
P5VS5_ITH_RC
R7625 22K 5% 1/16W MF-LF 402
C7630 0.1uF 20% 16V CERM 402
C7607 0.01uF 10% 16V CERM 402
XW7600 SM
TP_P5V_P1V5_PGOOD 65

P5VP1V5_SKIP
R7606 0 5% 1/16W MF-LF 402
P5VP1V5_FCB
P5VP1V5_CONT
R7607 0 5% 1/16W MF-LF 402
PP5V_S5 67 66 65 64 63 61 51 46 25 5 70
C7605 1uF 10% 6.3V CERM 402
C7601 4.7uF 20% 6.3V CERM 603
C7602 1uF 10% 6.3V CERM 402
PP5V_S5_P5VP1V5_INTVCC 61
VOLTAGE=5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
R7603 30K 5% 1/16W MF-LF 402
R7604 10K 5% 1/16W MF-LF 402
P5VP1V5_FSEL 61
C7604 0.01uF 10% 16V CERM 402

P1V5S0_BOOST_RC
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
R7664 0 5% 1/16W MF-LF 402
CRITICAL D7664 SOD-323 CMDSH-3
CRITICAL Q7660 FDM6296 MICROFET3X3
C7664 0.1uF 20% 10V CERM 402
CRITICAL Q7661 IRF7832PBF SO-8
NO STUFF C7661 1000pF 10% 25V X7R 402

C7662 0.001uF 10% 16V CERM 402
C7665 470pF 10% 50V CERM 402
C7666 100pF 5% 50V CERM 402
P1V5S0_ITH_RC
R7665 10K 5% 1/16W MF-LF 402
C7670 0.1uF 20% 16V CERM 402

C7663 0.1uF 10% 16V X5R 402
R7663 909 1% 1/16W MF-LF 402
R7660 3.65K 1% 1/16W MF-LF 402
C7660 0.1uF 10% 16V X5R 402
R7669 1.21K 1% 1/16W MF-LF 402
CRITICAL L7660 2.2uH-14A IHLP2525CZ-SM

PP1V5_S0_REG
Vout = 1.49V
8A max output
(L7660 & Q7660 limit)

C7690 22UF 20% 6.3V CERM 805
CRITICAL C7692 330uF 20% 2V POLY CASE-D2-SM
C7691 22UF 20% 6.3V CERM 805

<Ra>
C7667 470pF 10% 50V CERM 402
R7667 34.0K 1% 1/16W MF-LF 402

<Rb>
NO STUFF C7668 1000pF 10% 25V X7R 402
R7668 39.2K 1% 1/16W MF-LF 402

Vout = 0.8V * (1 + Ra / Rb)

5V S0 FET

Q7695 FDC638P SM-LF
PP5V_S5 67 66 65 64 63 61 51 46 25 5 70
C7695 0.0022uF 10% 16V CERM 402
C7696 22UF 20% 6.3V CERM 805
PP5V_S0 89 57 56 29 31 36 42 47 52 54 56 57 60 61 65 66 67 70 78 79 80
C7697 22UF 20% 6.3V CERM 805
R7695 100K 5% 1/16W MF-LF 402
PM_SLP_S3_LS5V 65 61 47 5
P5VS0_EN2_L_RC

5V S3 FET

Q7610 FDC638P SM-LF
PP5V_S5 67 66 65 64 63 61 51 46 25 5 70
PP5V_S3 5 45 51 66 80
C7610 0.0022uF 10% 16V CERM 402
R7610 100K 5% 1/16W MF-LF 402
PM_SLP_S4_LS5V 65 64
P5VS3_EN_L_RC

5V S0 FET

NO STUFF Q7615 FDC638P SM-LF
PP5V_S5 67 66 65 64 63 61 51 46 25 5 70
NO STUFF C7615 0.0022uF 10% 16V CERM 402
NO STUFF C7616 22UF 20% 6.3V CERM 805
PP5V_S0 4 5 25 31 36 42 47 52 54 56 57 60 61 65 66 67 70 78 79 80
NO STUFF CRITICAL C7618 150uF 20% 2V POLY CASE-D2-LF
NO STUFF C7617 22UF 20% 6.3V CERM 805
NO STUFF R7615 100K 5% 1/16W MF-LF 402
PM_SLP_S3_LS5V 65 61 47 5
P5VS0_EN_L_RC

5V / 1.5V Power Supply

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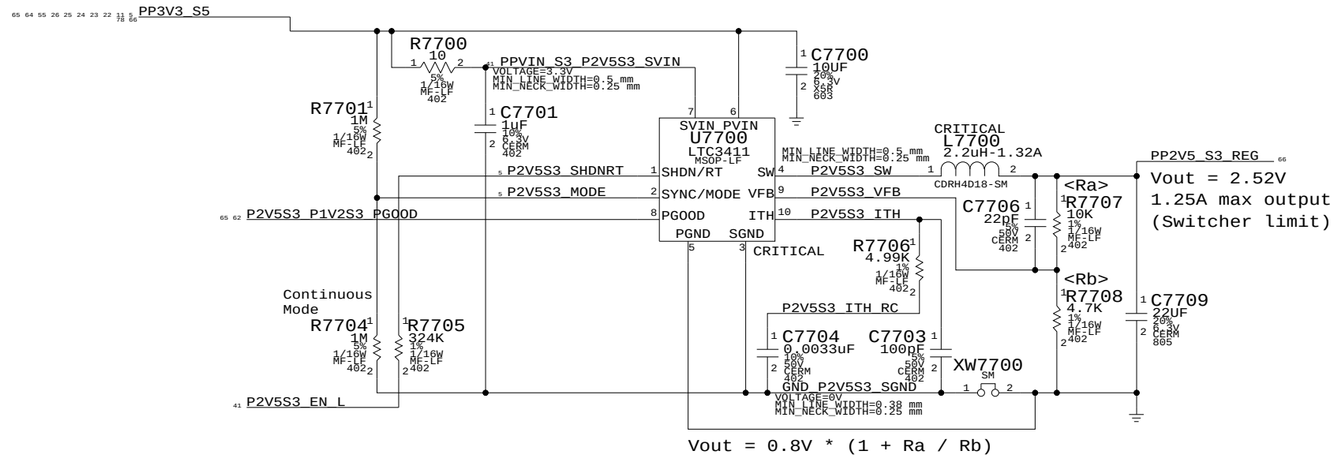
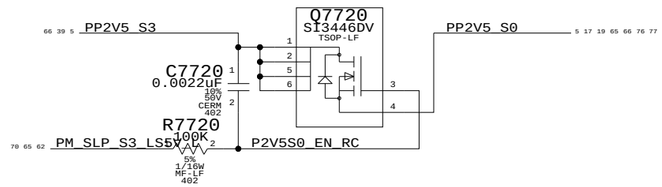
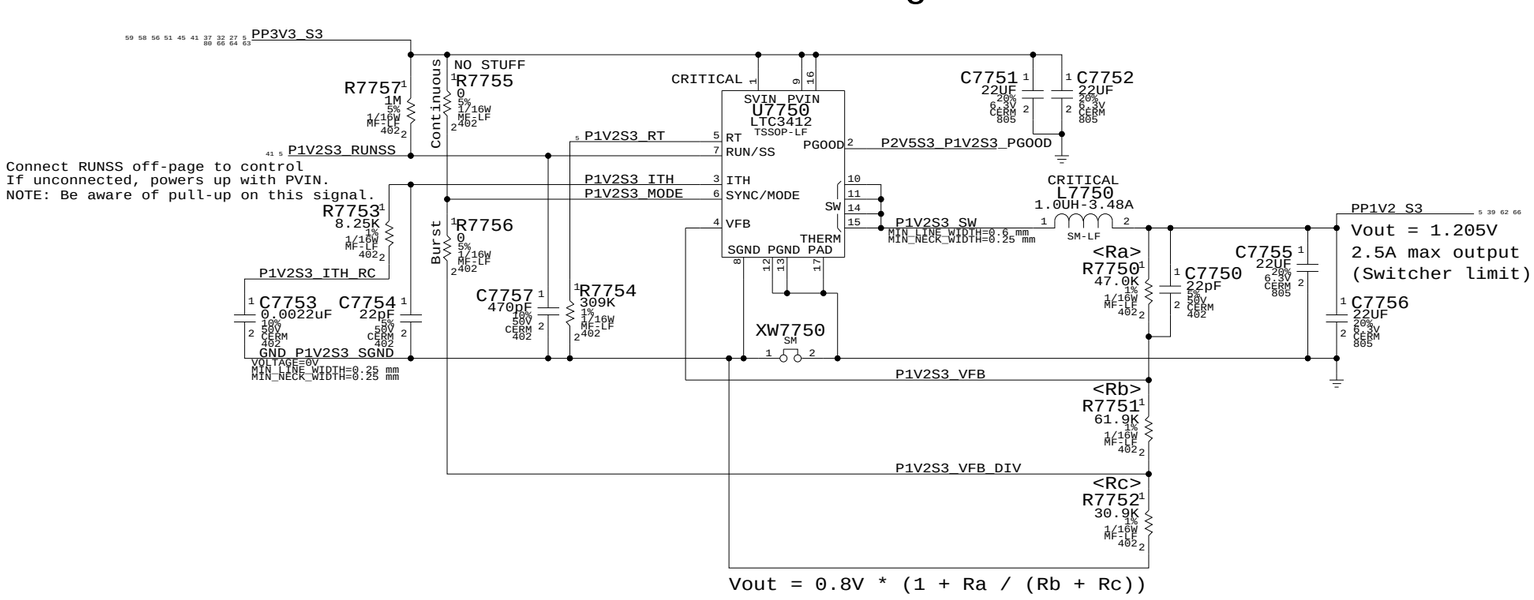
2.5V S3 Regulator



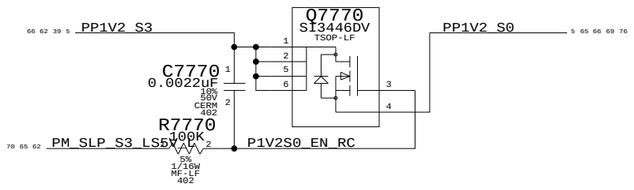
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



2.5V & 1.2V Regulators

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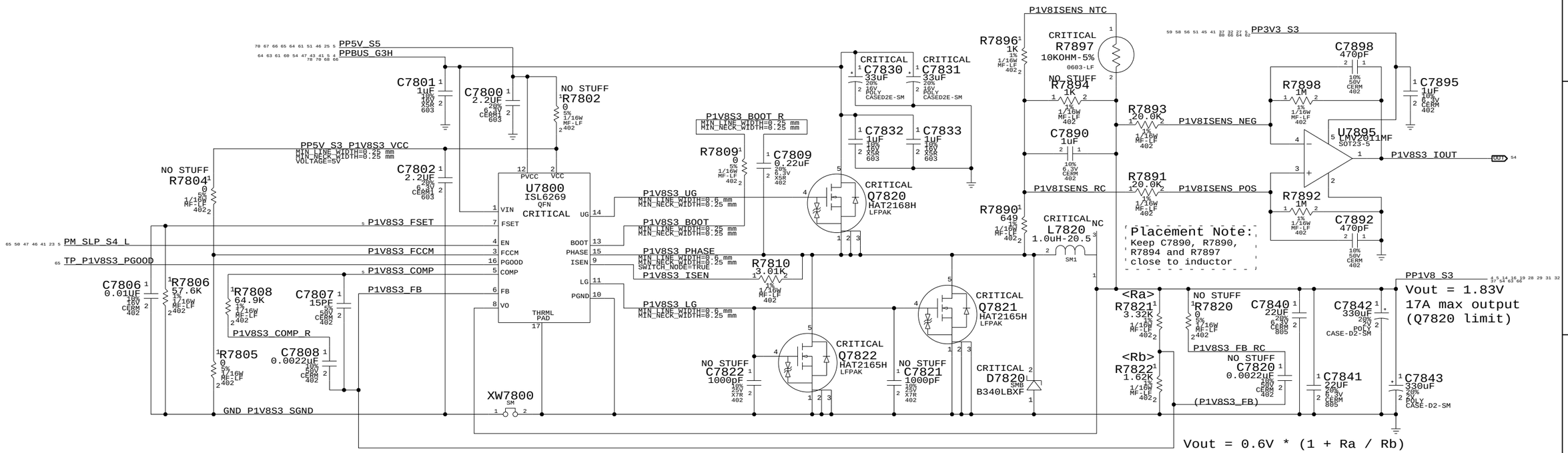
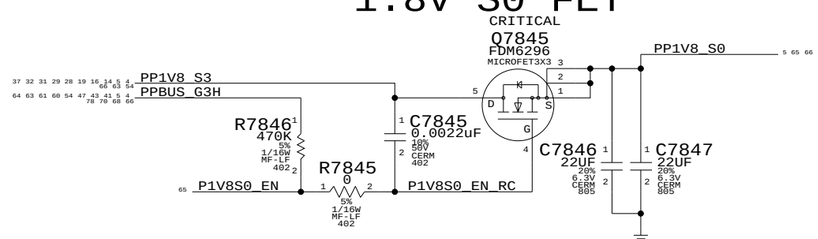
1.8V S3 Current Sense


PP5V_S5
PPBUS_G3H
PP5V_S3_P1V8S3_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
C7801 1uF 10V X5R 603
C7800 2.2UF 20% 6.3V CERM 603
NO STUFF R7802 0 5% 1/16W MF-LF 402
C7802 2.2UF 20% 6.3V CERM 603
NO STUFF R7804 0 5% 1/16W MF-LF 402
U7800 ISL6269 QFN CRITICAL
VIN FSET EN FCCM PGOOD COMP FB VO
PVCC VCC UG BOOT PHASE ISEN LG PGND
THRML PAD
XW7800 SM
P1V8S3_BOOT_R
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R7809 0 5% 1/16W MF-LF 402
C7809 0.22uF 20% 6.3V X5R 402
P1V8S3_UG
P1V8S3_BOOT
P1V8S3_PHASE
P1V8S3_ISEN
P1V8S3_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
R7810 3.01K 1% 1/16W MF-LF 402
CRITICAL C7830 33uF 20% 16V POLY CASED2E-SM
CRITICAL C7831 33uF 20% 16V POLY CASED2E-SM
C7832 1uF 10% 16V X5R 603
C7833 1uF 10% 16V X5R 603
CRITICAL Q7820 HAT2168H LFPAK
CRITICAL Q7821 HAT2165H LFPAK
CRITICAL Q7822 HAT2165H LFPAK
NO STUFF C7822 1000pF 10% 25V X7R 402
NO STUFF C7821 1000pF 10% 25V X7R 402
CRITICAL D7820 SMB B340LBXF
P1V8S3_FSET
P1V8S3_FCCM
P1V8S3_COMP
P1V8S3_FB
P1V8S3_COMP_R
PM_SLP_S4_L
TP_P1V8S3_PGOOD
C7806 0.01UF 10% 16V CERM 402
R7806 57.6K 1% 1/16W MF-LF 402
R7808 64.9K 1% 1/16W MF-LF 402
C7807 15PF 5% 50V CERM 402
R7805 0 5% 1/16W MF-LF 402
C7808 0.0022uF 10% 25V CERM 402
GND_P1V8S3_SGND
P1V8ISENS_NTC
R7896 1K 1% 1/10W MF-LF 402
CRITICAL R7897 10KOHM-5% 0603-LF
NO STUFF R7894 1K 1% 1/10W MF-LF 402
R7893 20.0K 1% 1/10W MF-LF 402
C7890 1uF 10% 6.3V CERM 402
P1V8ISENS_NEG
P1V8ISENS_RC
P1V8ISENS_POS
R7891 20.0K 1% 1/10W MF-LF 402
R7890 649 1% 1/10W MF-LF 402
CRITICAL L7820 1.0uH-20.5 SM1
NC
Placement Note:
Keep C7890, R7890, R7894 and R7897 close to inductor
PP3V3_S3
C7898 470pF 10% 50V CERM 402
R7898 1M 1% 1/10W MF-LF 402
C7895 1uF 10% 6.3V CERM 402
U7895 LMV2011MF SOT23-5
P1V8S3_IOUT
R7892 1M 1% 1/10W MF-LF 402
C7892 470pF 10% 50V CERM 402
PP1V8_S3
Vout = 1.83V
17A max output
(Q7820 limit)
<Ra> R7821 3.32K 1% 1/16W MF-LF 402
NO STUFF R7820 0 5% 1/16W MF-LF 402
C7840 22UF 20% 6.3V CERM 805
C7842 330uF 20% 2V POLY CASE-D2-SM
P1V8S3_FB_RC
NO STUFF C7820 0.0022uF 10% 25V CERM 402
C7841 22UF 20% 6.3V CERM 805
C7843 330uF 20% 2V POLY CASE-D2-SM
<Rb> R7822 1.62K 1% 1/16W MF-LF 402
(P1V8S3_FB)
Vout = 0.6V * (1 + Ra / Rb)

1.8V S0 FET



1.8V Supply

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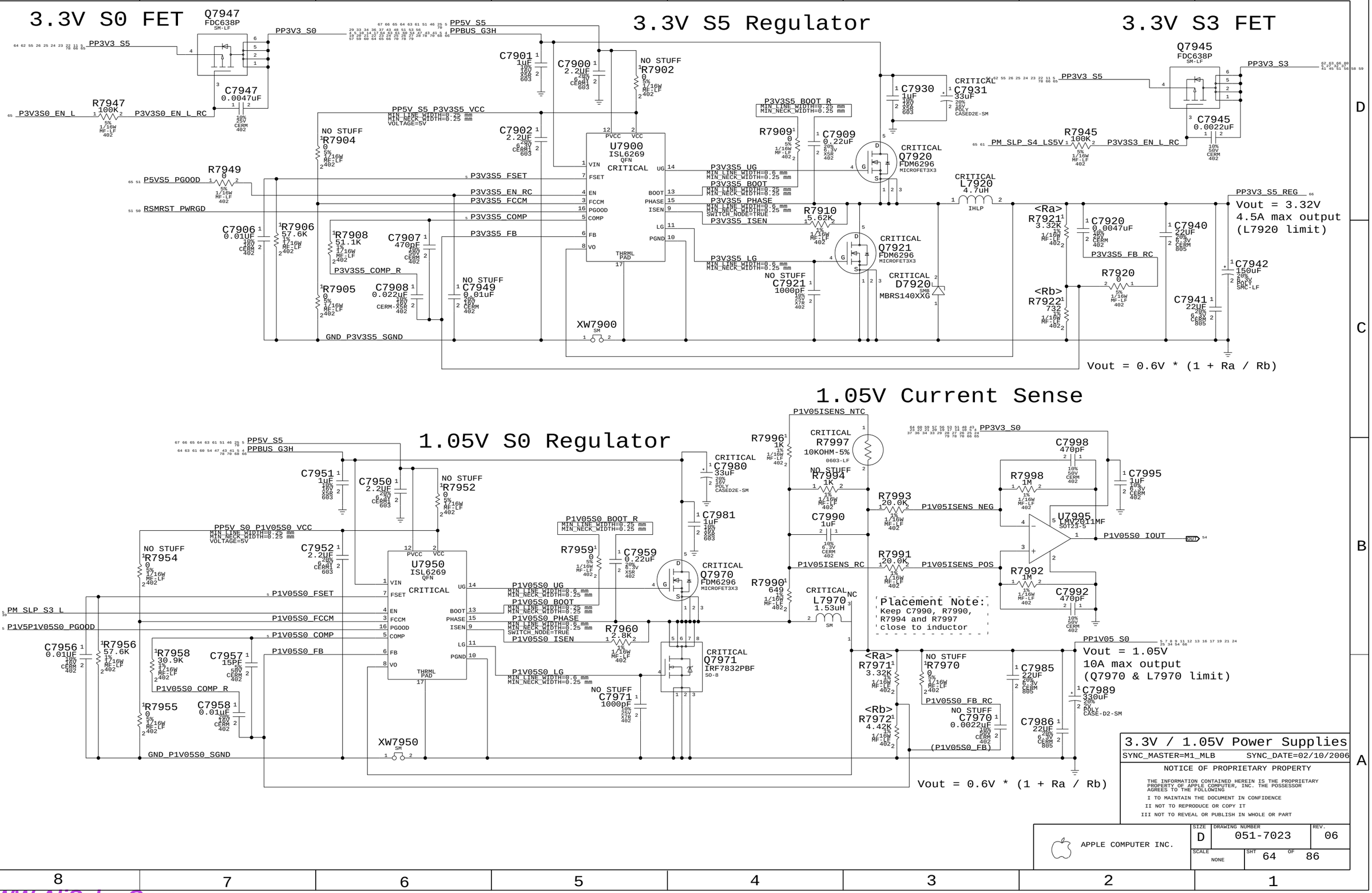

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Power Control Signals

PP5V_S5

R8050 10K 5% 1/10W MF-LF 402
R8051 10K 5% 1/10W MF-LF 402
R8052 10K 5% 1/10W MF-LF 402

PM_SLP_S3_LS5V_L

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

PM_SLP_S3_LS5V_L (MAKE_BASE=TRUE) → PM_SLP_S3_LS5V_L
P3V3S0_EN_L (MAKE_BASE=TRUE) → P3V3S0_EN_L
P1V8S0_EN (MAKE_BASE=TRUE) → P1V8S0_EN

1.8V Enable has pull-up to PBUS

Q8055 2N7002DW-X-F SOT-363
Q8056 2N7002DW-X-F SOT-363
Q8050 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V (MAKE_BASE=TRUE) → PM_SLP_S3_LS5V

PP3V42_G3H

Q8050 2N7002DW-X-F SOT-363
R8054 100K 5% 1/10W MF-LF 402
Q8057 2N7002DW-X-F SOT-363

P1V5S0_RUNSS

1.5V Enable has pull-up to PBUS

Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3

PM_SLP_S3_L

R8056 100K 5% 1/10W MF-LF 402

(PM_SLP_S3_L) (MAKE_BASE=TRUE) → PM_SLP_S3_L

R8053 10K 5% 1/16W MF-LF 402

P2V5S3_P1V2S3_PGOOD
P2V5S3_P1V2S3_PGOOD

NO STUFF
R8060 0 5% 1/16W MF-LF 402

P2V5S3_P1V2S3_PGOOD (MAKE_BASE=TRUE) → GPUVCORE_EN (MAKE_BASE=TRUE) → GPUVCORE_EN

Ensure 1.2V and 2.5V S3 supplies are up before enabling GPU VCore to support removing ethernet power in battery sleep.

PP5V_S5

R8055 10K 5% 1/10W MF-LF 402

PM_SLP_S4_LS5V (MAKE_BASE=TRUE) → PM_SLP_S4_LS5V

Q8055 2N7002DW-X-F SOT-363

PM_SLP_S4_L

R8057 100K 5% 1/10W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L) (MAKE_BASE=TRUE) → PM_SLP_S4_L

PP3V42_G3H

P5VS5_PGOOD

(P5VS5_PGOOD) (MAKE_BASE=TRUE) → P5VS5_PGOOD

R8059 470K 5% 1/10W MF-LF 402

P5VS5_RUNSS

5V Enable has pull-up to PBUS

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN_L

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN

R8058 100K 5% 1/10W MF-LF 402

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

PPDCIN_G3H

C8000 10uF 10% 25V X5R 1206

U8000 LT3470 TSOT23-8
VIN BOOST SHDN* SW BIAS NC FB GND

P3V42G3H5_BOOST
C8005 0.22uF 10% 6.3V X5R 402
CRITICAL L8010 33uH CDPH4D19F-SM
P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE

NC CRITICAL

C8010 22pF 5% 50V CERM 402

<Ra> R8010 348K 1% 1/16W MF-LF 402
<Rb> R8011 200K 1% 1/16W MF-LF 402

P3V42G3H_FB

PP3V42_G3H
Vout = 3.425
200mA max output (Switcher limit)

C8015 22UF 20% 6.3V CERM 805

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

PP3V3_S5
PP1V5_S0

R8061 27.4K 1% 1/10W MF-LF 402
R8063 4.99K 1% 1/16W MF-LF 402

C8060 0.1uF 10% 16V CERM 402

U8060 LMC7211 SM-LF

0.89V Reference → P1V0_P1V5PG_REF

P1V5S0_COMP_POS

R8062 10K 1% 1/10W MF-LF 402
R8064 10K 1% 1/16W MF-LF 402

1.5V Comp threshold set to 1.32V (88%)

P1V5S0_PGOOD → R8065 10K 5% 1/16W MF-LF 402

P1V5P1V05S0_PGOOD (OUT)

P1V5P1V05S0_PGOOD (IN)

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8065 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

TP_P5V_P1V5_PGOOD — TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)
TP_P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation

PP5V_S0
PP3V3_S0
PP2V5_S0
PP1V8_S0
PP1V2_S0
PP0V9_S0

C8070 0.1uF 10% 16V CERM 402
C8071 0.1uF 10% 16V CERM 402

U8070 LTC2908 LLP
V1 V2 V3 V4 CRITICAL VADJ1 VADJ2 RST* GND THRML PAD

R8074 68.1K 1% 1/10W MF-LF 402
R8072 124K 1% 1/16W MF-LF 402
R8075 100K 1% 1/10W MF-LF 402
R8073 100K 1% 1/16W MF-LF 402

S0PGOOD_1V2_DIV
S0PGOOD_0V9_DIV

S0PGOOD_PWROK → R8076 549K 1% 1/16W MF-LF 402

LTC2908 sources 6uA at 5.0V
R8076 serves as pull-down
and 3.3V level-shifter.

LTC2908 threshold is 95% (4.75V, 3.135V, 2.375V, 1.71V, 1.14V, 0.86V)

PP3V3_S0 → MC74VHC1G08 SC70 U8080 → ALL_SYS_PWRGD (OUT)

C8080 0.1uF 10% 16V CERM 402

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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"S3AC" rail is ON in S3 on AC, OFF in S3 on battery

PP0V9_S0
PP1V05_S0
PP1V2_S3
PP1V2_S0
PP1V5_S0_REG
PP1V5_S0
PP3V3_S3
PP1V8_S3
PP1V8_S0
PP2V5_S3_REG
PP2V5_S3
PP2V5_S0
PPVCORE_S0_GPU
PPDCIN_G3H
GND
PP3V42_G3H
PP3V3_S5_REG
PP3V3_S5
PP3V3_S0
PP1V8_S0_GPU
PP3V3_S0_GPU
PP3V3_S3AC
PNBB_S0_GPU
PPBB_S0_GPU
PPVCORE_S0_CPU
PPBUS_G3H
PPBUS_S5_FW_FET
PP5V_S5_REG
PP5V_S5
PP5V_S3
PP5V_S0

XW8115 JUMPER OPEN
XW8133 JUMPER OPEN
XW8119 JUMPER OPEN
XW8125 JUMPER OPEN
XW8150 JUMPER OPEN

R8133 0 5% 1/8W MF-LF 805

PLACEMENT_NOTE=Place on top-side of board

Power Aliases

SYNC_MASTER=M1_MLB SYNC_DATE=12/19/2005

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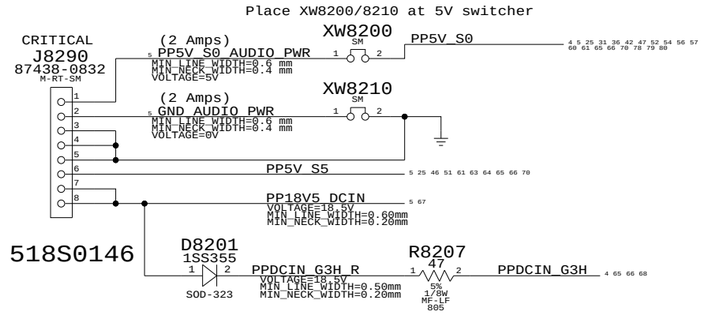
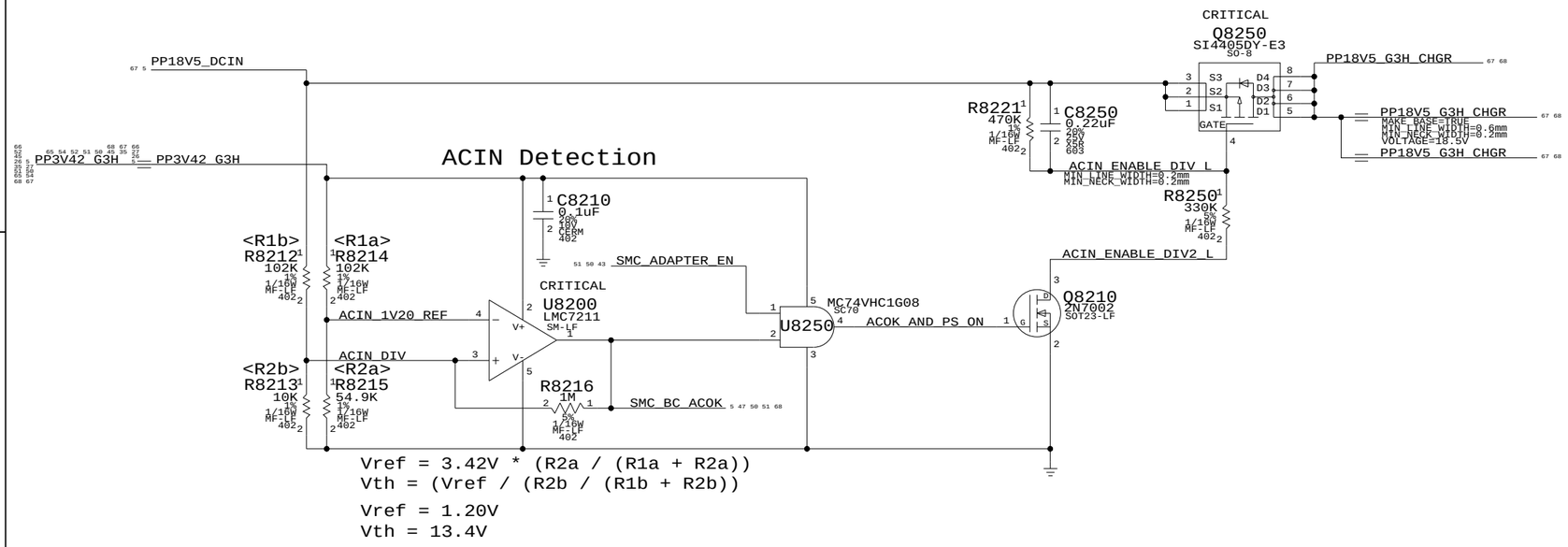
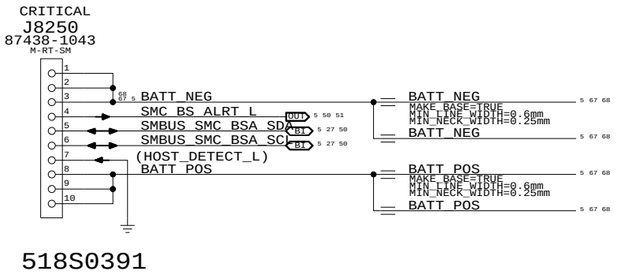
DC-In Connector



Inrush Limiter



Battery Connector



DC-In & Battery Connectors			
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)		
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PBUS SUPPLY

PP18V5_G3H_CHGR
Q8340 IRLML5203-2.6A SM
CHGR_VDD
CHGR_DCIN
R8342 93.1K 1% 1/10W MF-LF 402
R8340 118K 1% 1/16W MF-LF 402
R8341 10K 1% 1/16W MF-LF 402
D8340 MMBD914XXG SOT23
CHGR_ACSET
CHGR_CSON_R
R8343 10K 1% 1/16W MF-LF 402
CHGR_ACSET_D
R8344 100K 1% 1/16W MF-LF 402
C8340 0.1uF 20% 25V CERM 402
C8341 0.1uF 10% 16V CERM 402
CHGR_SGND
CHGR_DCSET
C8300 0.033uF 10% 16V X5R 402
NO STUFF C8307 0.1UF 20% 25V CERM 603
R8311 0 5% 1/16W MF-LF 402
C8301 0.022uF 10% 16V CERAMIC X5R 402
R8301 34.8K 1% 1/16W MF-LF 402
NO STUFF C8314 0.068UF 10% 16V CERM 402
NO STUFF C8315 680pF 10% 50V CERM 402
C8302 0.0082uF 10% 25V X7R 402
C8311 1uF 10% 6.3V CERM 402
C8319 0.0033uF 10% 25V CERM 402
R8302 100 1% 1/16W MF-LF 402
R8300 4.7 5% 1/10W MF-LF 402
C8312 1uF 10% 6.3V CERM 402
CHGR_SGND
CHGR_VDD
CHGR_VDDP
CHGR_ICOMP_R
CHGR_ICM
CHGR_VCOMP_C1
U8300 ISL6255AHRZ QFN
ICM 5
ACLIM 8
ICOMP 3
VCOMP 4
VADJ 9
CELLS 2
CSOP 21
CSON 22
CHLIM 7
VREF 6
ACPRN 23
ACSET 27
THRML_PAD 29
GND 10
PGND 11
VDD 26
VDDP 13
SGATE 18
CSIP 19
CSIN 20
BGATE 17
DCIN 25
BOOT 14
UGATE 15
PHASE 16
LGATE 12
EN 1
DCPRN 24
DCSET 28
CHGR_ACLIM
CHGR_ICOMP
CHGR_VCOMP
CHGR_VADJ
CHGR_CSO_P
CHGR_CSO_N
CHGR_CHLIM
CHGR_VREF
CHGR_ACPRN
CHGR_ACSET
CHGR_SGATE
CHGR_CSI_P
CHGR_CSI_N
NC_CHGR_BGATE
NO_TEST=TRUE
CHGR_DCIN
CHGR_BOOT
CHGR_UGATE
CHGR_LGATE
CHGR_EN
CHGR_DCPRN
CHGR_DCSET
CRITICAL Q8300 SI4405DY-E3 SO-8
D4 D3 D2 D1 S3 S2 S1 GATE
PPVDCIN_G3H_PRE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
NO STUFF R8310 100K 1% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.2mm
MIN_NECK_WIDTH=0.2mm
XW8301 SM
R8307 0.02 0.5% 1W MF 0612
C8304 0.1UF 20% 16V CERM 402
R8305 10 1% 1/16W MF-LF 402
CHGR_CSIN_R
XW8302 SM
PPVDCIN_G3H_R
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
C8316 10UF 20% 16V X5R 1206
C8305 10UF 20% 16V X5R 1206
C8306 10UF 20% 16V X5R 1206
R8303 2.2 5% 1/16W MF-LF 402
D8300 SOD-123 B0530WXF
C8303 0.1UF 20% 25V 402
CRITICAL Q8301 HAT2168H LFPAK
L8300 4.7UH SM
NC
10A max, limited by L8300, Q8301
PPBUS_G3H
CRITICAL C8308 33uF 20% 16V POLY CASED2E-SM
C8309 100uF 20% 16V ELEC 6.3X5.5SM1
R8308 0.01 0.5% 1W MF 0612
PPVBAT_G3H_CHGR_OUT
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
C8310 1uF 10% 16V X5R 603
XW8304 SM
XW8303 SM
0.5%
R8304 270 5% 1/16W MF-LF 402
CHGR_CSON_R
CHGR_CSO_N
R8306 2.2 5% 1/16W MF-LF 402
CHGR_CSOP_R
CHGR_CSO_P
R8370 49.9 1% 1/16W MF 603
CHGR_PHASE
SWITCH_NODE=TRUE
C8370 0.0022uF 10% 50V CERM 603
CRITICAL Q8302 HAT2165H LFPAK
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm

BATTERY CHARGER

CHGR_VDD
R8352 100K 1% 1/16W MF-LF 402
R8350 100K 1% 1/16W MF-LF 402
CHGR_EN
Q8350 2N7002 SOT23-LF
CHGR_SGND
CHGR_ACPRN
CHGR_DCPRN
CHGR_VREF
NO STUFF R8364 0 5% 1/16W MF-LF 402
CHGR_VADJ
NO STUFF R8365 0 5% 1/16W MF-LF 402
CHGR_SGND
If stuffed, R8364+R8365 > 70K so Iref < 100uA
CRITICAL Q8320 SI4405DY-E3 SO-8
CRITICAL Q8321 SI4405DY-E3 SO-8
R8320 27 5% 3W MF 2525
D8321 1SS355 SOD-323
PPVBATT_G3H_PRE
PPVBATT_G3H_DIO
VOLTAGE=12.6V
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.25mm
R8321 47 5% 1/8W MF-LF 805
PPDCIN_G3H
CRITICAL F8302 8AMP-24V 1206
PPVBATT_G3H_FET
PPVBATT_G3H_FUSE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.25mm
L8320 FERR-50-OHM SM-LF
BATT_POS
C8327 0.001UF 10% 50V CERM 402
GND_BATT_CHGND
C8330 0.001UF 10% 50V CERM 402
L8321 FERR-50-OHM SM-LF
BATT_NEG
PPVBAT_G3H_CHGR_OUT
C8320 0.01uF 10% 16V CERM 402
C8321 0.1uF 10% 16V X5R 402
NO STUFF C8322 0.01UF 10% 16V CERM 402
C8325 0.22UF 10% 16V CERM 402
R8330 470K 1% 1/16W MF-LF 402
CHG_EN_DIV_L
MIN_LINE_WIDTH=0.2mm
MIN_NECK_WIDTH=0.2mm
R8322 39.2K 1% 1/16W MF-LF 402
TCHG_EN_DIV_L
MIN_LINE_WIDTH=0.2mm
MIN_NECK_WIDTH=0.2mm
R8331 330K 1% 1/16W MF-LF 402
NO STUFF C8324 0.01UF 20% 16V CERM 402
R8323 35.7K 1% 1/16W MF-LF 402
CHG_EN_DIV2_L
TCHG_EN_DIV2_L
SMC_SYS_ISET
R8360 10K 1% 1/16W MF-LF 402
R8363 11K 1% 1/16W MF-LF 402
C8361 0.1UF 20% 16V CERM 402
CHGR_ACLIM
CHGR_SGND
Using PWM drive
PP3V42_G3H
R8324 100K 1% 1/16W MF-LF 402
CHGR_ACPRN
Q8322 2N7002DW-X-F SOT-363
Q8324 2N7002DW-X-F SOT-363
SMC_BC_ACOK
R8325 10K 1% 1/16W MF-LF 402
SMC_BC_ACOK_R
C8323 0.1UF 20% 16V CERM 402
SMC_BATT_CHG_EN
SMC_BATT_TRICKLE_EN_L
CHGR_VREF
R8367 24.3K 1% 1/16W MF-LF 402
SMC_BATT_ISET
R8362 24.3K 1% 1/16W MF-LF 402
R8366 6.04K 1% 1/16W MF-LF 402
C8362 0.1UF 10% 16V CERM 402
CHGR_CHLIM
As shown, Ichg = 3.9A max
CHGR_SGND
Using PWM drive

PBus Supply & Batt. Charger
SYNC_MASTER=M1_LIO
SYNC_DATE=12/19/2005

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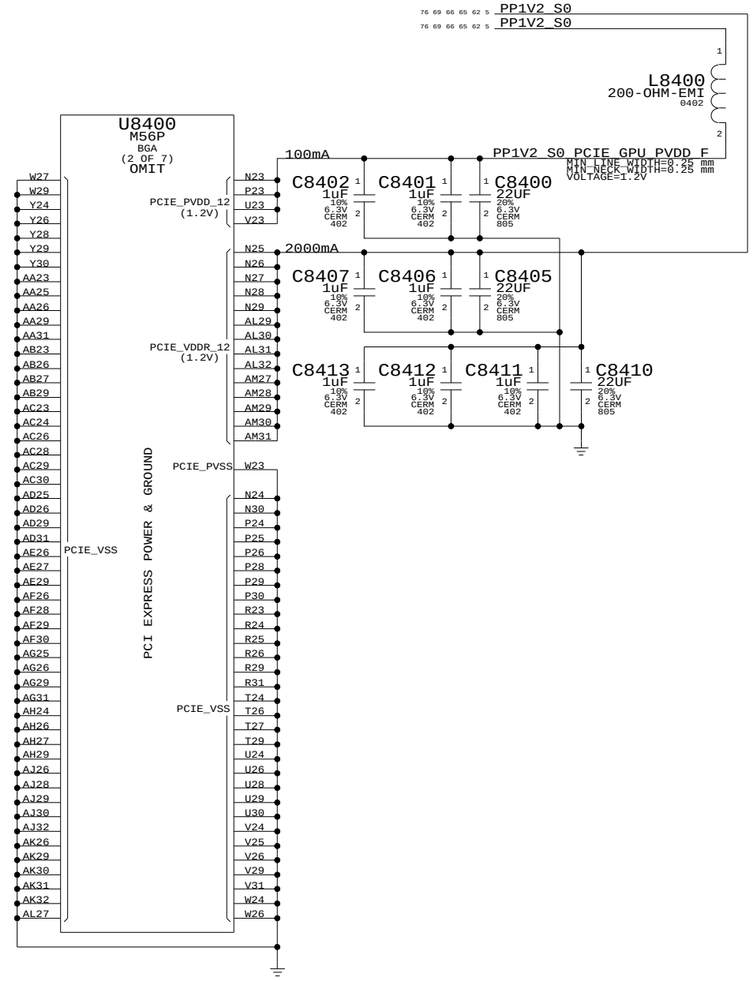

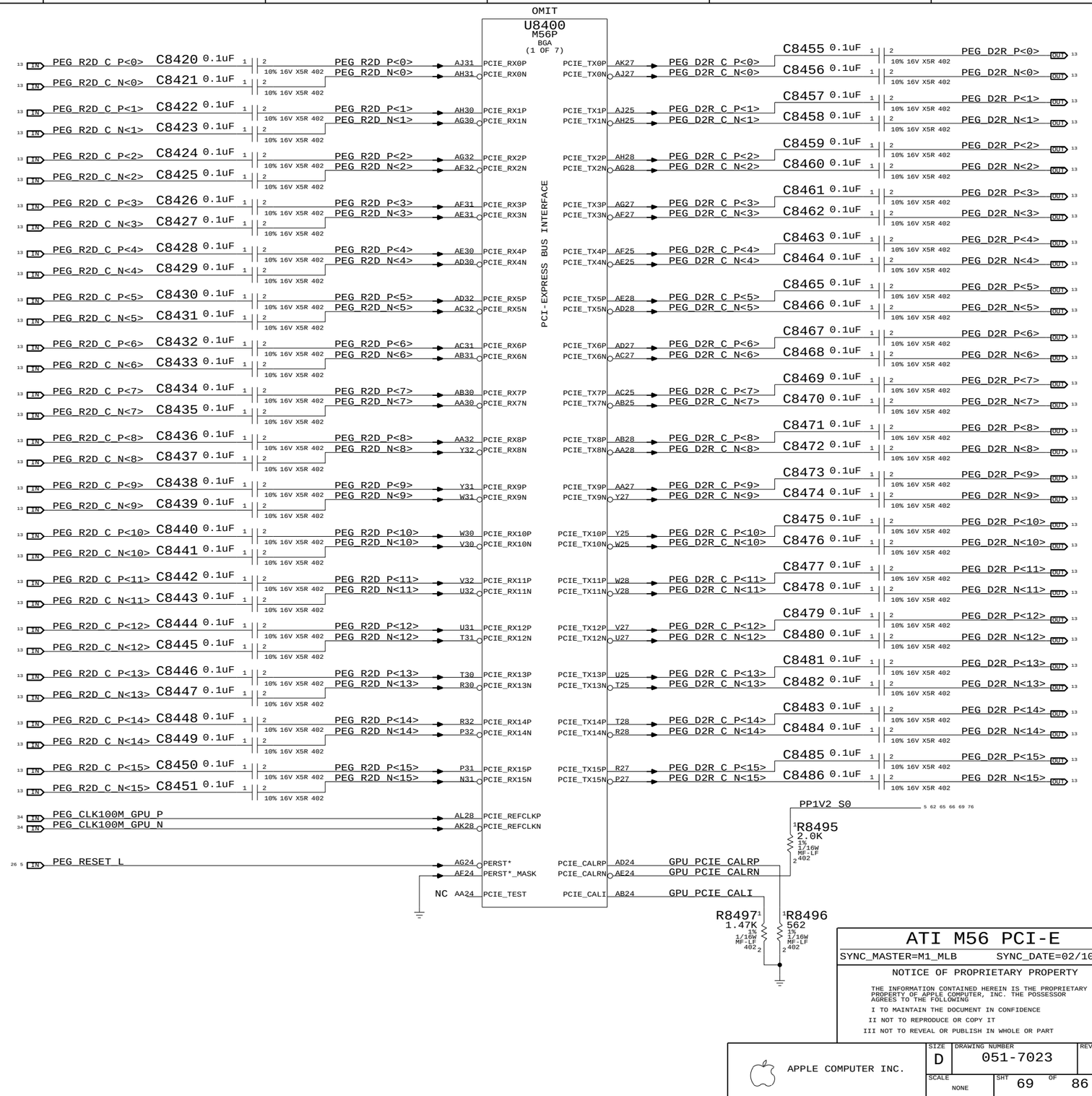

ATI M56 PCI-E

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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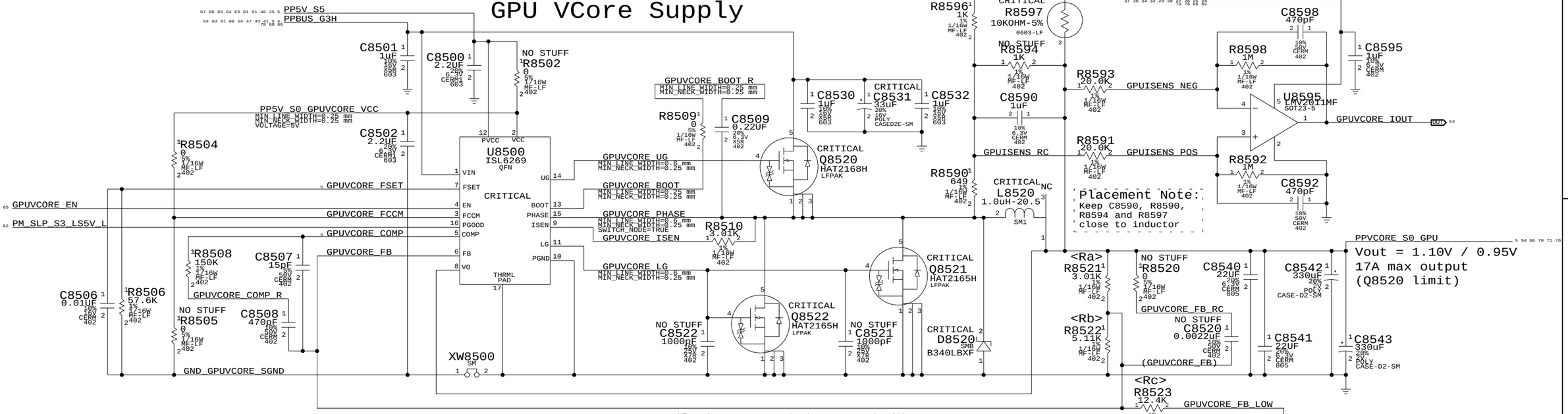
GPU VCore Supply

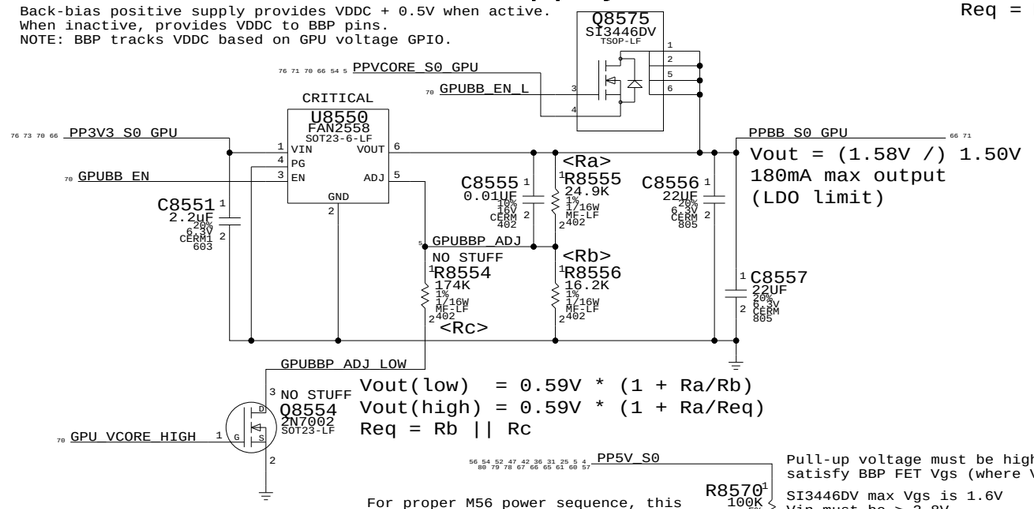

PP5V_S5
PPBUS_G3H
C8501 1uF 10% 16V X5R 603
C8500 2.2UF 20% 6.3V CERM1 603
NO STUFF R8502 0 5% 1/16W MF-LF 402
PP5V_S0_GPUVCORE_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
C8502 2.2UF 20% 6.3V CERM1 603
R8504 0 5% 1/16W MF-LF 402
GPUVCORE_EN
PM_SLP_S3_LS5V_L
GPUVCORE_FSET
GPUVCORE_FCCM
GPUVCORE_COMP
GPUVCORE_FB
GPUVCORE_COMP_R
R8508 150K 1% 1/16W MF-LF 402
C8507 15pF 5% 50V CERM 402
C8506 0.01UF 10% 16V CERM 402
R8506 57.6K 1% 1/16W MF-LF 402
NO STUFF R8505 0 5% 1/16W MF-LF 402
C8508 470pF 10% 50V CERM 402
GND_GPUVCORE_SGND
XW8500 SM
CRITICAL U8500 ISL6269 QFN
VIN FSET EN FCCM PGOOD COMP FB VO PVCC VCC UG BOOT PHASE ISEN LG PGND THRML PAD
GPUVCORE_BOOT_R
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R8509 0 5% 1/16W MF-LF 402
C8509 0.22UF 20% 6.3V X5R 402
GPUVCORE_UG
GPUVCORE_BOOT
GPUVCORE_PHASE
SWITCH_NODE=TRUE
GPUVCORE_ISEN
GPUVCORE_LG
R8510 3.01K 1% 1/16W MF-LF 402
C8530 1uF 10% 16V X5R 603
CRITICAL C8531 33uF 20% 16V POLY CASED2E-SM
C8532 1uF 10% 16V X5R 603
CRITICAL Q8520 HAT2168H LFPAK
CRITICAL Q8521 HAT2165H LFPAK
NO STUFF C8522 1000pF 10% 25V X7R 402
NO STUFF C8521 1000pF 10% 25V X7R 402
CRITICAL Q8522 HAT2165H LFPAK
CRITICAL D8520 SMB B340LBXF
GPUISENS_NTC
R8596 1K 1% 1/16W MF-LF 402
CRITICAL R8597 10KOHM-5% 0603-LF
NO STUFF R8594 1K 1% 1/16W MF-LF 402
C8590 1uF 10% 6.3V CERM 402
R8593 20.0K 1% 1/16W MF-LF 402
GPUISENS_NEG
GPUISENS_RC
R8591 20.0K 1% 1/16W MF-LF 402
GPUISENS_POS
R8590 649 1% 1/16W MF-LF 402
CRITICAL L8520 1.0uH-20.5 SM1
NC
Placement Note:
Keep C8590, R8590, R8594 and R8597 close to inductor
PP3V3_S0
C8598 470pF 10% 50V CERM 402
R8598 1M 1% 1/16W MF-LF 402
C8595 1uF 10% 6.3V CERM 402
U8595 LMV2011MF SOT23-5
GPUVCORE_IOUT
R8592 1M 1% 1/16W MF-LF 402
C8592 470pF 10% 50V CERM 402
PPVCORE_S0_GPU
Vout = 1.10V / 0.95V
17A max output
(Q8520 limit)
<Ra> R8521 3.01K 1% 1/16W MF-LF 402
<Rb> R8522 5.11K 1% 1/16W MF-LF 402
NO STUFF R8520 0 5% 1/16W MF-LF 402
GPUVCORE_FB_RC
NO STUFF C8520 0.0022UF 10% 16V CERM 402
(GPUVCORE_FB)
C8540 22UF 20% 6.3V CERM 805
C8542 330uF 20% 2V POLY CASE-D2-SM
C8541 22UF 20% 6.3V CERM 805
C8543 330uF 20% 2V POLY CASE-D2-SM
<Rc> R8523 12.4K 1% 1/16W MF-LF 402
GPUVCORE_FB_LOW

Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

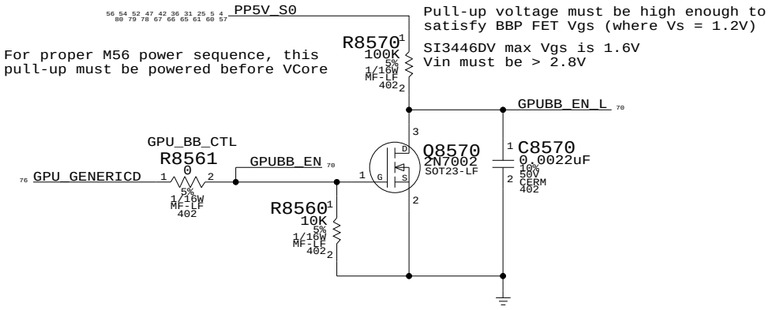
GPU VCore Current Sense

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



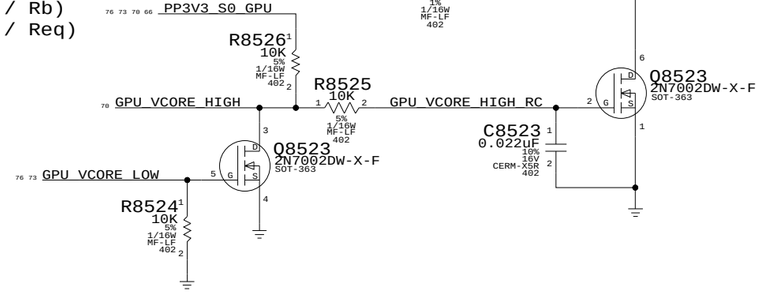
Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc



For proper M56 power sequence, this pull-up must be powered before VCore

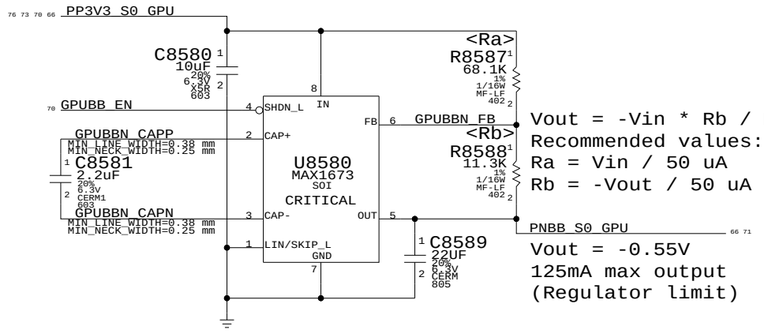
Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)

SI3446DV max Vgs is 1.6V
Vin must be > 2.8V



Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.



Vout = -Vin * Rb / Ra
Recommended values:
Ra = Vin / 50 uA
Rb = -Vout / 50 uA

Vout = -0.55V
125mA max output
(Regulator limit)

GPU (M56) Core Supplies		
SYNC_MASTER=M1_MLB	SYNC_DATE=02/10/2006	
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	SCALE NONE	SHT 70 OF 86

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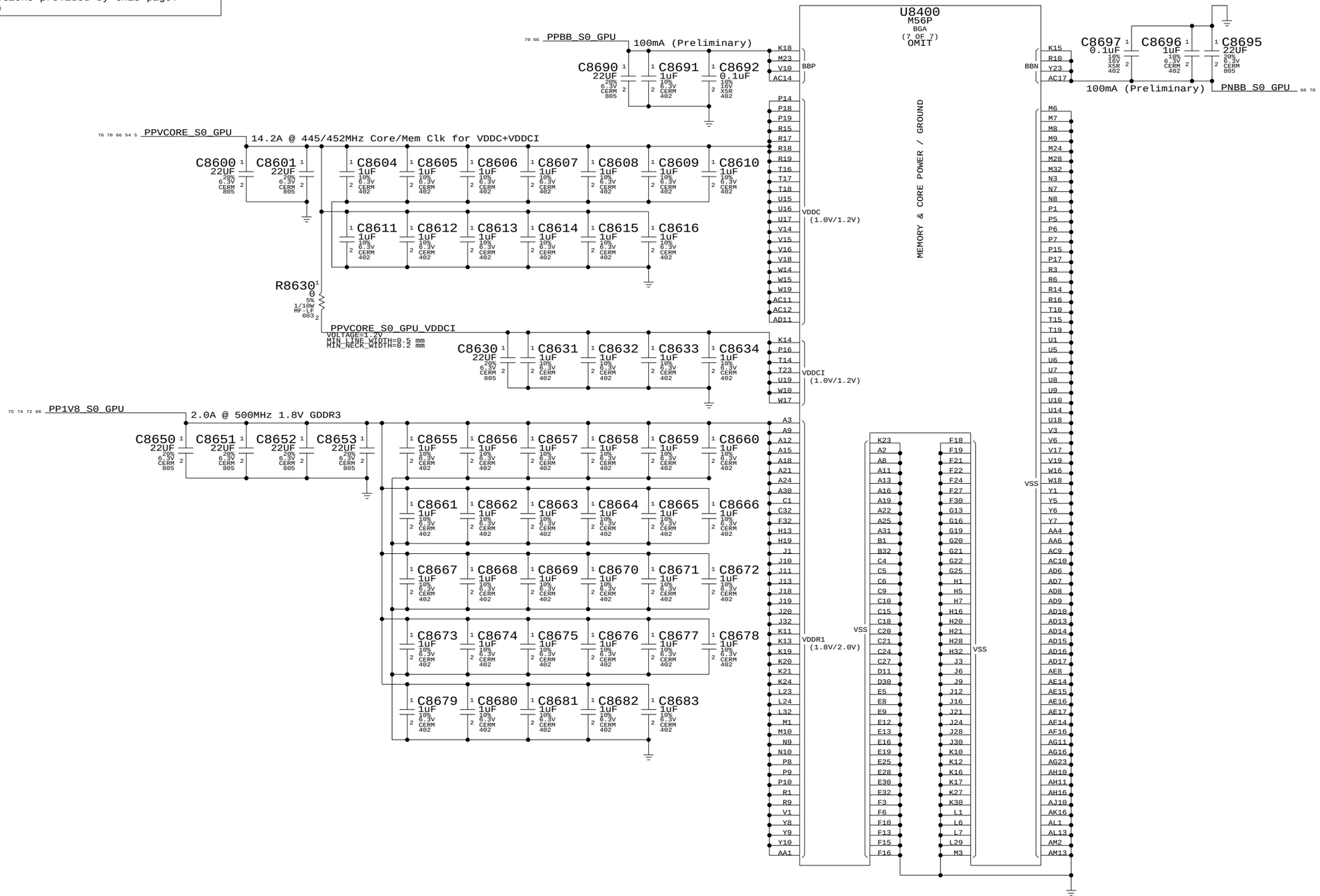
Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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NONE	71	86

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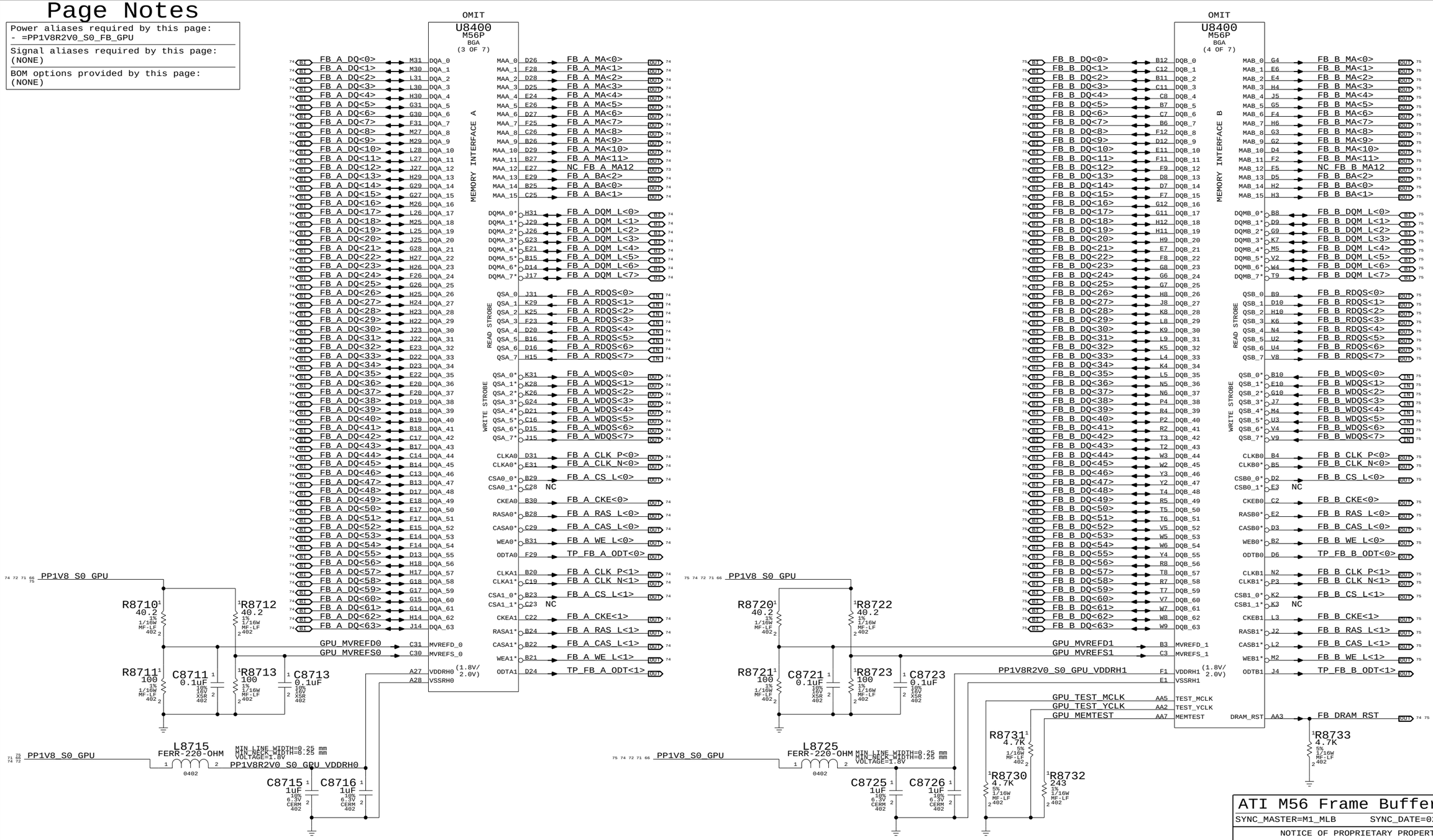
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE NONE SHT 72 OF 86

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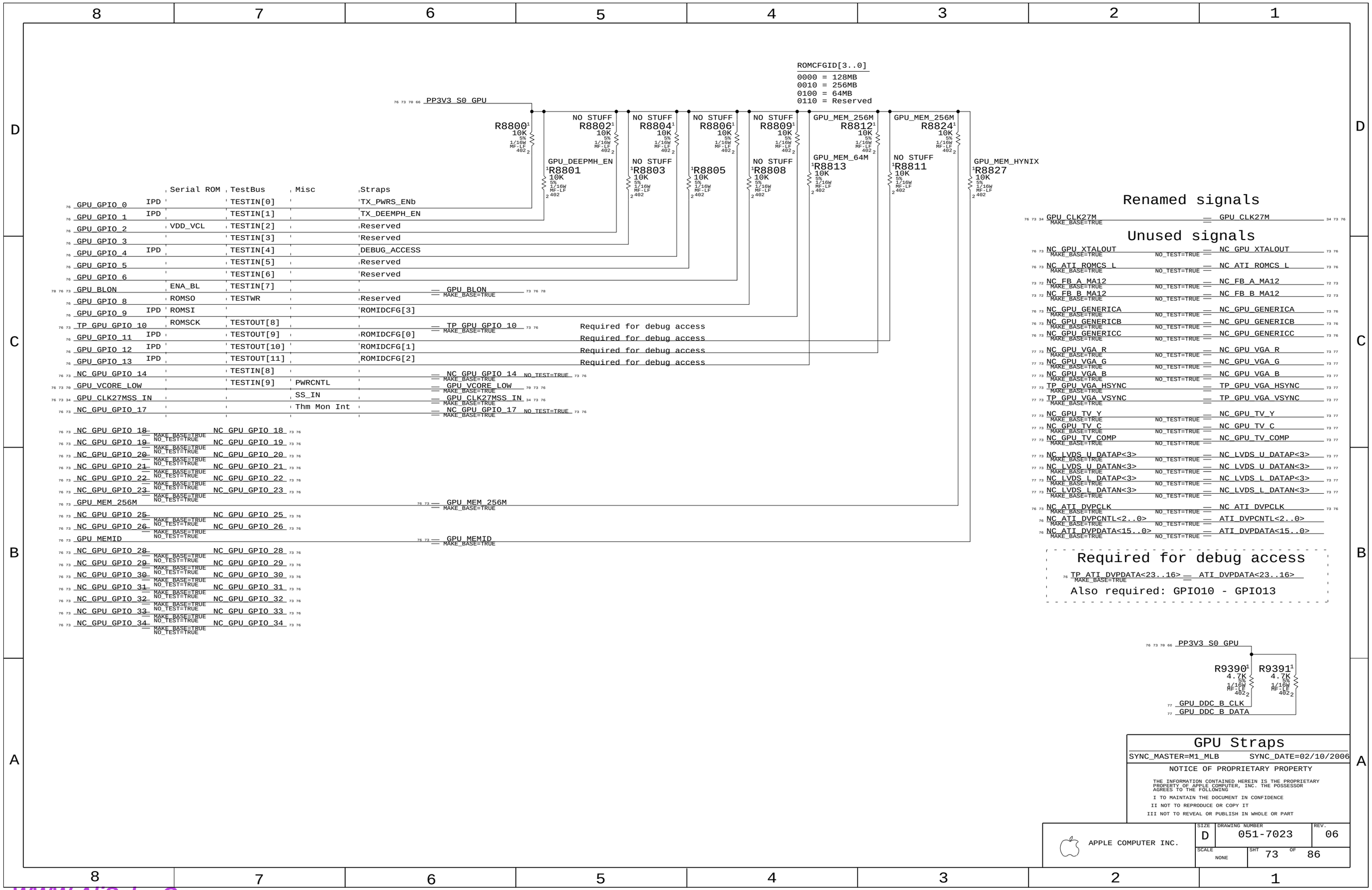

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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

Connect to designated pin, then GND

Connect to designated pin, then GND

SYNC_MASTER=M1_MLB	SYNC_DATE=02/10/2006

GDDR3 Frame Buffer A

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D	051-7023	06
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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

CRITICAL
OMIT

U9000
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U9050
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

PP1V8_S0_GPU

Connect to designated pin, then GND

L9010 FERR-220-OHM
PP1V8_S0_FB_B0_VDDA0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

L9015 FERR-220-OHM
PP1V8_S0_FB_B0_VDDA1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

L9060 FERR-220-OHM
PP1V8_S0_FB_B1_VDDA0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

L9065 FERR-220-OHM
PP1V8_S0_FB_B1_VDDA1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

FB_B0_VREF0
FB_B0_VREF1
FB_B1_VREF0
FB_B1_VREF1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

FB_B0_ZQ
FB_B0_MF
FB_B0_SEN
FB_B1_ZQ
FB_B1_MF
FB_B1_SEN

FB_DRAM_RST

FB_B_MA<0>
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FB_B_MA<2>
FB_B_MA<3>
FB_B_MA<4>
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FB_B_DQ<58>
FB_B_DQ<57>

GDDR3 Frame Buffer B

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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SCALE: NONE

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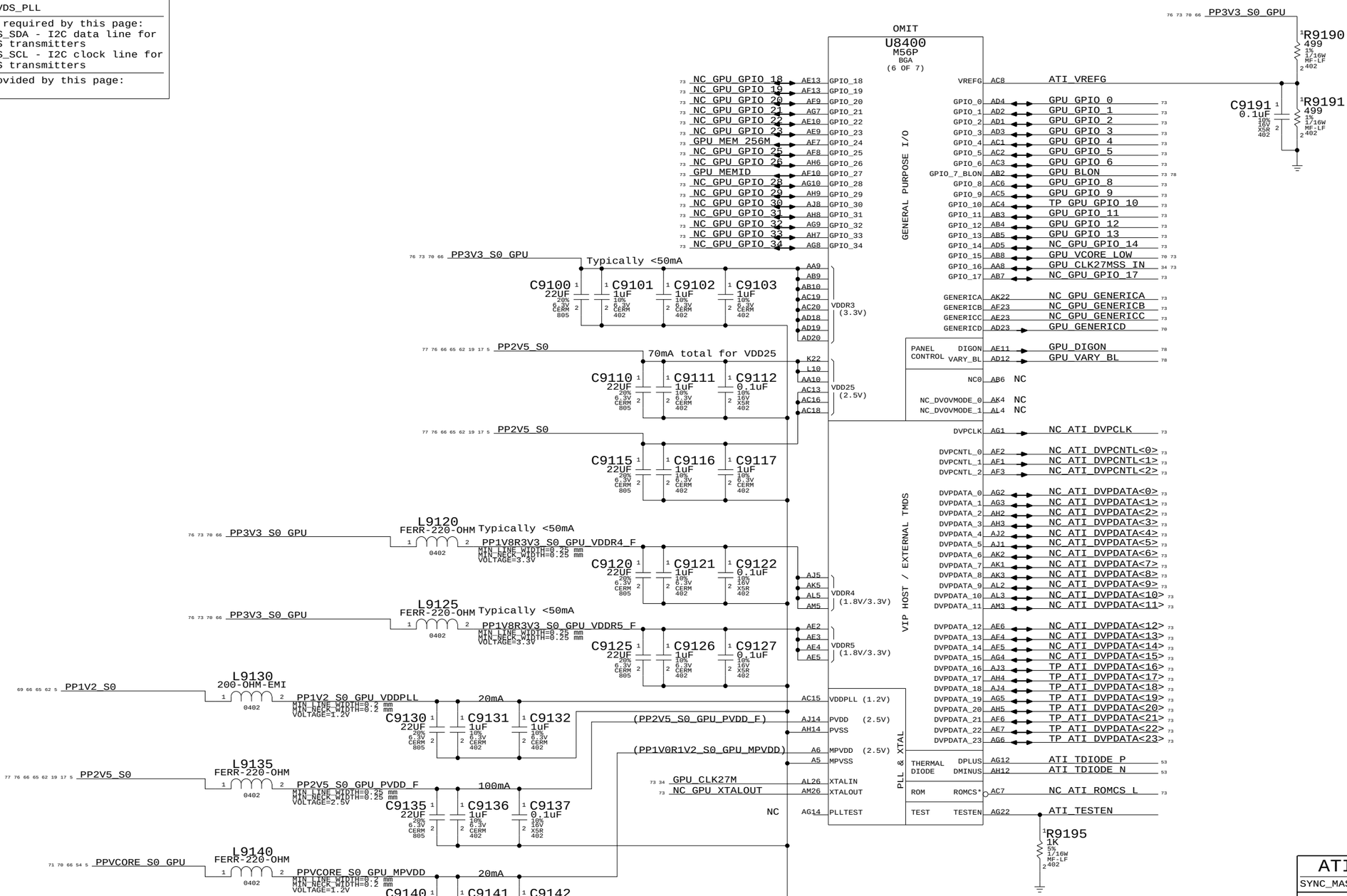
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



NC_GPU_GPIO_18	AE13	GPIO_18	
NC_GPU_GPIO_19	AF13	GPIO_19	
NC_GPU_GPIO_20	AF9	GPIO_20	
NC_GPU_GPIO_21	AG7	GPIO_21	
NC_GPU_GPIO_22	AE10	GPIO_22	
NC_GPU_GPIO_23	AE9	GPIO_23	
GPU_MEM_256M	AF7	GPIO_24	
NC_GPU_GPIO_25	AF8	GPIO_25	
NC_GPU_GPIO_26	AH6	GPIO_26	
GPU_MEMID	AF10	GPIO_27	
NC_GPU_GPIO_28	AG10	GPIO_28	
NC_GPU_GPIO_29	AH9	GPIO_29	
NC_GPU_GPIO_30	AJ8	GPIO_30	
NC_GPU_GPIO_31	AH8	GPIO_31	
NC_GPU_GPIO_32	AG9	GPIO_32	
NC_GPU_GPIO_33	AH7	GPIO_33	
NC_GPU_GPIO_34	AG8	GPIO_34	

VREFG	AC8	ATI_VREFG	
GPIO_0	AD4	GPU_GPIO_0	73
GPIO_1	AD2	GPU_GPIO_1	73
GPIO_2	AD1	GPU_GPIO_2	73
GPIO_3	AD3	GPU_GPIO_3	73
GPIO_4	AC1	GPU_GPIO_4	73
GPIO_5	AC2	GPU_GPIO_5	73
GPIO_6	AC3	GPU_GPIO_6	73
GPIO_7_BLON	AB2	GPU_BLON	73 78
GPIO_8	AC6	GPU_GPIO_8	73
GPIO_9	AC5	GPU_GPIO_9	73
GPIO_10	AC4	TP_GPU_GPIO_10	73
GPIO_11	AB3	GPU_GPIO_11	73
GPIO_12	AB4	GPU_GPIO_12	73
GPIO_13	AB5	GPU_GPIO_13	73
GPIO_14	AD5	NC_GPU_GPIO_14	73
GPIO_15	AB8	GPU_VCORE_LOW	70 73
GPIO_16	AA8	GPU_CLK27MSS_IN	34 73
GPIO_17	AB7	NC_GPU_GPIO_17	73
GENERICA	AK22	NC_GPU_GENERICA	73
GENERICB	AF23	NC_GPU_GENERICB	73
GENERICC	AE23	NC_GPU_GENERICC	73
GENERICD	AD23	GPU_GENERICD	70
PANEL CONTROL DIGON	AE11	GPU_DIGON	78
PANEL CONTROL VARY_BL	AD12	GPU_VARY_BL	78
NC0	AB6	NC	
NC_DVOVMODE_0	AK4	NC	
NC_DVOVMODE_1	AL4	NC	
DVPCLK	AG1	NC_ATI_DVPCLK	73
DVPCNTL_0	AF2	NC_ATI_DVPCNTL<0>	73
DVPCNTL_1	AF1	NC_ATI_DVPCNTL<1>	73
DVPCNTL_2	AF3	NC_ATI_DVPCNTL<2>	73
DVPDATA_0	AG2	NC_ATI_DVPDATA<0>	73
DVPDATA_1	AG3	NC_ATI_DVPDATA<1>	73
DVPDATA_2	AH2	NC_ATI_DVPDATA<2>	73
DVPDATA_3	AH3	NC_ATI_DVPDATA<3>	73
DVPDATA_4	AJ2	NC_ATI_DVPDATA<4>	73
DVPDATA_5	AJ1	NC_ATI_DVPDATA<5>	73
DVPDATA_6	AK2	NC_ATI_DVPDATA<6>	73
DVPDATA_7	AK1	NC_ATI_DVPDATA<7>	73
DVPDATA_8	AK3	NC_ATI_DVPDATA<8>	73
DVPDATA_9	AL2	NC_ATI_DVPDATA<9>	73
DVPDATA_10	AL3	NC_ATI_DVPDATA<10>	73
DVPDATA_11	AM3	NC_ATI_DVPDATA<11>	73
DVPDATA_12	AE6	NC_ATI_DVPDATA<12>	73
DVPDATA_13	AF4	NC_ATI_DVPDATA<13>	73
DVPDATA_14	AF5	NC_ATI_DVPDATA<14>	73
DVPDATA_15	AG4	NC_ATI_DVPDATA<15>	73
DVPDATA_16	AJ3	TP_ATI_DVPDATA<16>	73
DVPDATA_17	AH4	TP_ATI_DVPDATA<17>	73
DVPDATA_18	AJ4	TP_ATI_DVPDATA<18>	73
DVPDATA_19	AG5	TP_ATI_DVPDATA<19>	73
DVPDATA_20	AH5	TP_ATI_DVPDATA<20>	73
DVPDATA_21	AF6	TP_ATI_DVPDATA<21>	73
DVPDATA_22	AE7	TP_ATI_DVPDATA<22>	73
DVPDATA_23	AG6	TP_ATI_DVPDATA<23>	73
THERMAL DIODE DPLUS	AG12	ATI_TDIODE_P	53
THERMAL DIODE DMINUS	AH12	ATI_TDIODE_N	53
ROM ROMCS*	AC7	NC_ATI_ROMCS_L	73
TEST TESTEN	AG22	ATI_TESTEN	

PP1V2_S0			
VDDPLL	AC15	VDDPLL (1.2V)	
PVDD	AJ14	(2.5V)	
PVSS	AH14		
MPVDD	A6	(2.5V)	
MPVSS	A5		
GPU_CLK27M	AL26	XTALIN	34
NC_GPU_XTALOUT	AM26	XTALOUT	73
NC	AG14	PLLTEST	

PP3V3_S0_GPU			
PP2V5_S0			
PP1V8R3V3_S0_GPU_VDDR4_F			
PP1V8R3V3_S0_GPU_VDDR5_F			
PP1V2_S0			
PP1V2_S0_GPU_VDDPLL			
PP2V5_S0_GPU_PVDD_F			
PP1V0R1V2_S0_GPU_MPVDD			
PPVCORE_S0_GPU			
PPVCORE_S0_GPU_MPVDD			

ATI M56 GPIO/DVO/Misc

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PP2V5_S0
Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9300 22UF 20% 6.3V CERM 805; C9301 1UF 10% 6.3V CERM 402; C9302 1UF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
C9305 22UF 20% 6.3V CERM 805; C9306 1UF 10% 6.3V CERM 402; C9307 0.1UF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
C9310 22UF 20% 6.3V CERM 805; C9311 1UF 10% 6.3V CERM 402; C9312 0.1UF 10% 16V X5R 402

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9315 22UF 20% 6.3V CERM 805; C9316 1UF 10% 6.3V CERM 402; C9317 0.1UF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
C9320 22UF 20% 6.3V CERM 805; C9321 1UF 10% 6.3V CERM 402; C9322 0.1UF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9325 22UF 20% 6.3V CERM 805; C9326 1UF 10% 6.3V CERM 402; C9327 0.1UF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9330 22UF 20% 6.3V CERM 805; C9331 1UF 10% 6.3V CERM 402; C9332 1UF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.35 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
C9340 22UF 20% 6.3V CERM 805; C9345 22UF 20% 6.3V CERM 805; C9341 1UF 10% 6.3V CERM 402; C9342 0.1UF 10% 16V X5R 402; C9346 0.1UF 10% 16V X5R 402; C9347 0.1UF 10% 16V X5R 402

OMIT
U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
- AM8 TPVDD (2.5V)
- AL8 TPVSS
- AJ6, AK6, AL6, AM6 TXVDDR (2.5V)
- AJ7, AK7, AK8, AL7, AM7 TXVSSR

DAC (CRT)
- AL25, AM25 AVDD (2.5V)
- AJ24, AK25 AVSS
- AK23 AVSSQ
- AM23 VDD1DI (2.5V)
- AL23 VSS1DI
- 77 ATI RSET → AL22 RSET

DAC2 (TV/CRT2)
- AL16, AM16 A2VDD (2.5V)
- AL17, AM17 A2VSS
- NC AL14 NC_A2VDDQ
- AK13 A2VSSQ
- AJ16 VDD2DI (2.5V)
- AJ17 VSS2DI
- 77 ATI R2SET → AK14 R2SET

LVDS
- AE19, AE18 LPVDD (2.5V), LPVSS
- AC21, AC22, AD21, AD22, AE20, AE21, AE22, AF19, AF20 LVDDR (2.5V)
- AF17, AF18, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17 LVSSR

MONITOR IDENTIFICATION
- 79 LN GPU_HPD → AF11 HPD1

TMDS outputs:
- TXCP AM9 TMDS_CLK_P (OUT) 78 79 86
- TXCM AL9 TMDS_CLK_N (OUT) 78 79 86
- TX0P AL10 TMDS_DATA0_P (OUT) 79
- TX0M AK10 TMDS_DATA0_N (OUT) 79
- TX1P AM11 TMDS_DATA1_P (OUT) 79
- TX1M AL11 TMDS_DATA1_N (OUT) 79
- TX2P AM12 TMDS_DATA2_P (OUT) 79
- TX2M AL12 TMDS_DATA2_N (OUT) 79
- TX3P AJ9 TMDS_DATA3_P (OUT) 79
- TX3M AK9 TMDS_DATA3_N (OUT) 79
- TX4P AJ11 TMDS_DATA4_P (OUT) 79
- TX4M AK11 TMDS_DATA4_N (OUT) 79
- TX5P AJ12 TMDS_DATA5_P (OUT) 79
- TX5M AK12 TMDS_DATA5_N (OUT) 79

DAC (CRT) outputs:
- R AK24 NC_GPU_VGA_R (OUT) 73
- G AM24 NC_GPU_VGA_G (OUT) 73
- B AL24 NC_GPU_VGA_B (OUT) 73
- HSYNC AJ23 TP_GPU_VGA_HSYNC (OUT) 73
- VSYNC AJ22 TP_GPU_VGA_VSYNC (OUT) 73

DAC2 (TV/CRT2) outputs:
- R2 AK15 GPU_R2 (OUT) 78 79
- G2 AM15 GPU_G2 (OUT) 78 79
- B2 AL15 GPU_B2 (OUT) 78 79
- H2SYNC AF15 GPU_H2SYNC (OUT) 79
- V2SYNC AG15 GPU_V2SYNC (OUT) 79
- Y AJ15 NC_GPU_TV_Y (OUT) 73
- C AJ13 NC_GPU_TV_C (OUT) 73
- COMP AH15 NC_GPU_TV_COMP (OUT) 73

LVDS outputs:
- TXCLK_UP AJ21 LVDS_U_CLK_P (OUT) 78 81
- TXCLK_UN AK21 LVDS_U_CLK_N (OUT) 78 81
- TXOUT_U0P AG18 LVDS_U_DATA_P<0> (OUT) 78 81
- TXOUT_U0N AH18 LVDS_U_DATA_N<0> (OUT) 78 81
- TXOUT_U1P AK20 LVDS_U_DATA_P<1> (OUT) 78 81
- TXOUT_U1N AJ20 LVDS_U_DATA_N<1> (OUT) 78 81
- TXOUT_U2P AG20 LVDS_U_DATA_P<2> (OUT) 78 81
- TXOUT_U2N AH20 LVDS_U_DATA_N<2> (OUT) 78 81
- TXOUT_U3P AH21 NC_LVDS_U_DATAP<3> (OUT) 73
- TXOUT_U3N AG21 NC_LVDS_U_DATAN<3> (OUT) 73
- TXCLK_LP AM18 LVDS_L_CLK_P (OUT) 78 81
- TXCLK_LN AL18 LVDS_L_CLK_N (OUT) 78 81
- TXOUT_L0P AL19 LVDS_L_DATA_P<0> (OUT) 78 81
- TXOUT_L0N AK19 LVDS_L_DATA_N<0> (OUT) 78 81
- TXOUT_L1P AM20 LVDS_L_DATA_P<1> (OUT) 78 81
- TXOUT_L1N AL20 LVDS_L_DATA_N<1> (OUT) 78 81
- TXOUT_L2P AM21 LVDS_L_DATA_P<2> (OUT) 78 81
- TXOUT_L2N AL21 LVDS_L_DATA_N<2> (OUT) 78 81
- TXOUT_L3P AJ18 NC_LVDS_L_DATAP<3> (OUT) 73
- TXOUT_L3N AK18 NC_LVDS_L_DATAN<3> (OUT) 73

DDC outputs:
- DDC1CLK AH23 GPU_DDC_A_CLK (BI) 79
- DDC1DATA AH22 GPU_DDC_A_DATA (BI) 79
- DDC2CLK AG13 GPU_DDC_B_CLK (BI) 73
- DDC2DATA AH13 GPU_DDC_B_DATA (BI) 73
- DDC3CLK AF12 GPU_DDC_C_CLK (BI) 78
- DDC3DATA AE12 GPU_DDC_C_DATA (BI) 78

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI_RSET 77
ATI_R2SET 77
R9350 499 1% 1/16W MF-LF 402
R9351 715 1% 1/16W MF-LF 402

ATI M56 Video Interfaces

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
	VGA	VGA	GPU_R2
	VGA	VGA	GPU_G2
	VGA	VGA	GPU_B2
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_N<2..0>
	LVDS	LVDS	LVDS_U_CLK_P
	LVDS	LVDS	LVDS_U_CLK_N
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>
	LVDS	LVDS	LVDS_L_CLK_P
	LVDS	LVDS	LVDS_L_CLK_N
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>
	TMDS	TMDS	TMDS_CLK_P
	TMDS	TMDS	TMDS_CLK_N
	TMDS	TMDS	TMDS_DATA_P<5..3>
	TMDS	TMDS	TMDS_DATA_N<5..3>
	TMDS	TMDS	TMDS_DATA_P<2..0>
	TMDS	TMDS	TMDS_DATA_N<2..0>

PP3V3_S5
R9400 100K 5% 1/16W MF-LF 402
R9401 100K 5% 1/16W MF-LF 402
C9400 0.0022uF 10% 50V CERM 402
LCD_PWREN_L_RC
LCD_PWREN_L
Q9400 SI3443DV TSOP-LF
PP3V3_LCD_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V
L9400 FERR-250-OHM SM
C9401 0.001uF 10% 50V CERM 402
GND_CHASSIS_LVDS
Q9401 2N7002DW-X-F SOT-363
GPU_DIGON
R9494 100K 5% 1/16W MF-LF 402
PP3V3_S0
100K pull-ups are for no-panel case (development)
Panel has 2K pull-ups
R9410 100K 5% 1/16W MF-LF 402
R9411 100K 5% 1/16W MF-LF 402
GPU_DDC_C_CLK
GPU_DDC_C_DATA
C9410 0.001uF 10% 50V CERM 402
GND_CHASSIS_LVDS
GND_CHASSIS_LVDS
CRITICAL
J9400 MSC-RB30-5-FA F-RT-SM
C9420 0.001uF 10% 50V CERM 402
PP3V3_LCD_CONN MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=3.3V
NC
LVDS_L_DATA_N<0>
LVDS_L_DATA_P<0>
LVDS_L_DATA_CONN_N<1>
LVDS_L_DATA_CONN_P<1>
LVDS_L_DATA_CONN_N<2>
LVDS_L_DATA_CONN_P<2>
LVDS_L_CLK_N
LVDS_L_CLK_P
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_U_DATA_CONN_N<1>
LVDS_U_DATA_CONN_P<1>
LVDS_U_DATA_CONN_N<2>
LVDS_U_DATA_CONN_P<2>
LVDS_U_CLK_N
LVDS_U_CLK_P
C9421 0.001uF 20% 50V CERM 402
518S0289
GND_CHASSIS_LVDS

INVERTER INTERFACE

PPBUS_G3H
L9450 FERR-1K-OHM-EMI SM
PPBUS_S0_INVERTER MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=12.8V
C9450 0.001uF 20% 50V CERM 402
PP5V_S0
Q9450 FDG6332C_NL SC70-6 P-CHN
R9450 100K 5% 1/16W MF-LF 402
PP5V_INVERTER_SW_F MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V
L9452 400-OHM-EMI SM-1
C9451 10UF 20% 6.3V X5R 603
FP_PWR_EN_L
Q9450 FDG6332C_NL SC70-6 N-CHN
GPU_BLON
R9489 10K 5% 1/16W MF-LF 402
CRITICAL
J9450 SM-2MT-LF
NC
PP5V_INVERTER_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=5V
C9452 0.001uF 20% 50V CERM 402
NC
518S0293
L9454 400-OHM-EMI SM-1
INVERTER_PWM
GND_INVERTER MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=0V
C9454 0.001uF 20% 50V CERM 402
C9455 0.001uF 20% 50V CERM 402
L9455 60-OHM-EMI SM
GND_CHASSIS_INVERTER
PP3V3_S0
INVERTER_BUF
U9453 MC74VHC1G08 SC70
INVERTER_PWM_F
INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL
GPU_VARY_BL
INVERTER_BUF
C9453 0.1uF 20% 25V CERM 402
INVERTER_UNBUF
R9496 0 5% 1/16W MF-LF 402

Internal Display Connectors

SYNC_MASTER=M1_MLB SYNC_DATE=01/09/2006

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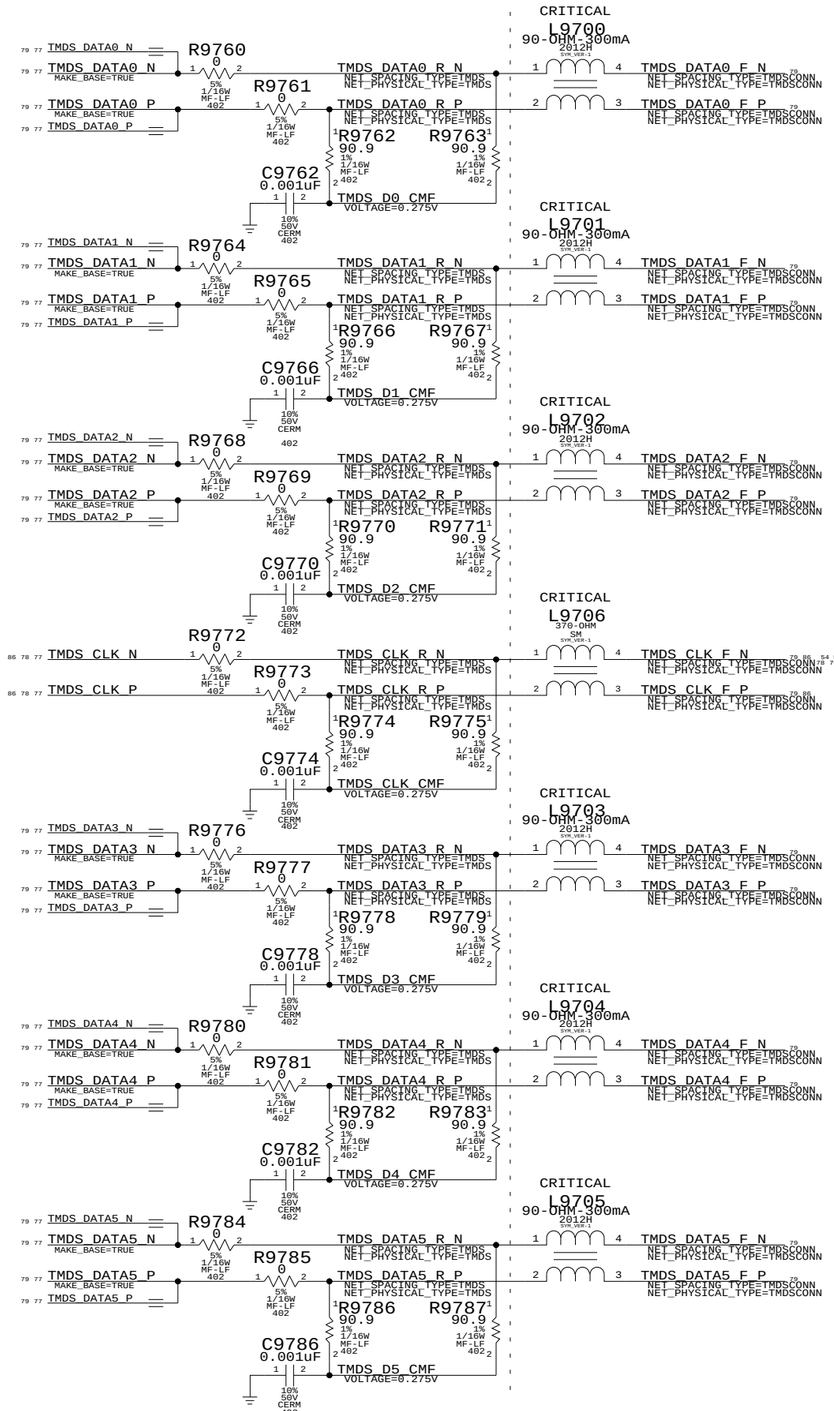
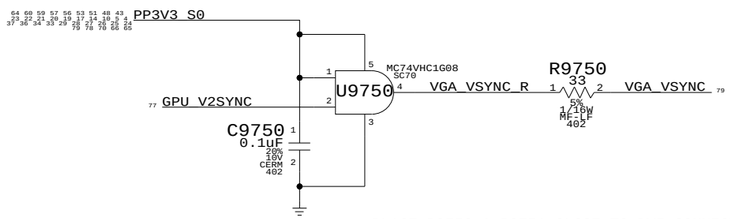
TMDS Filtering

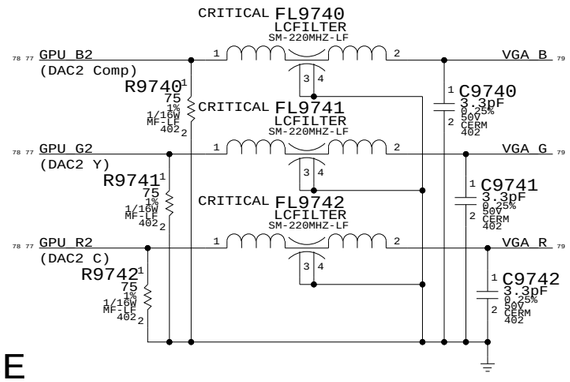
Place series R's and common-mode filtering close to GPU, common mode chokes near connector.



VGA SYNC BUFFERS

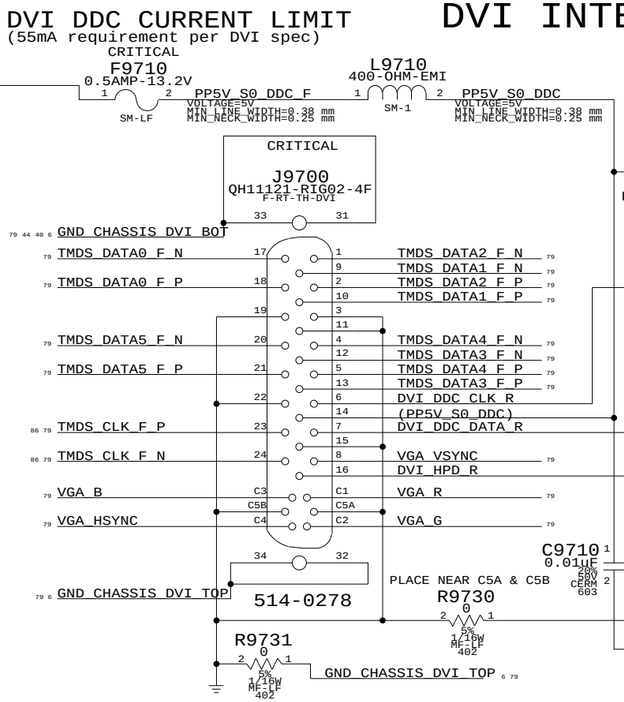


ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)



External Display Connector

SYNC_MASTER=M1_MLB SYNC_DATE=11/18/2005

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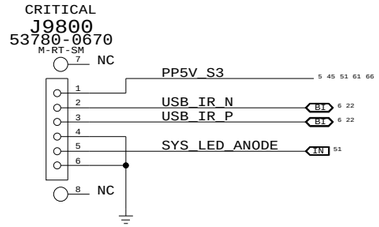
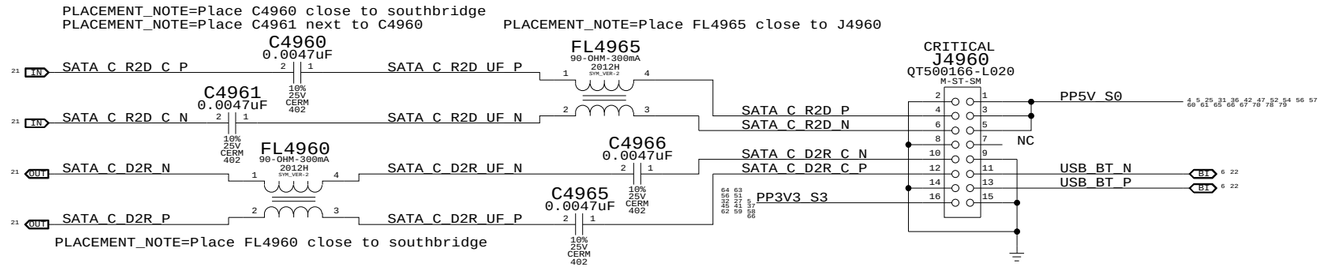
IR & Sleep LED Connector



518S0388

Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

M9 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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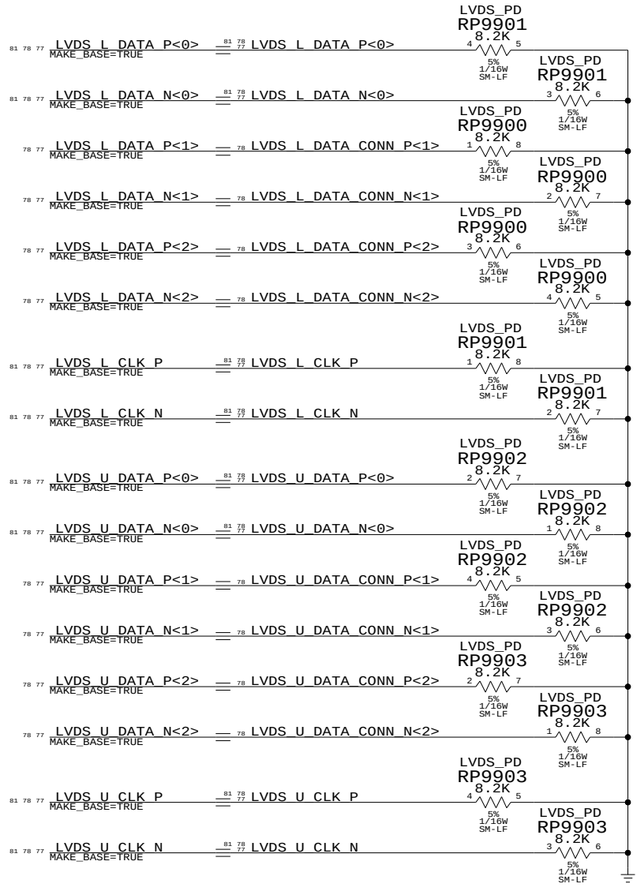
LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



LVDS Interface Pull-downs	
SYNC_MASTER=M1_MLB	SYNC_DATE=12/19/2005

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Revision History

Proto

11-29-05: -Release for Proto

11-30-05: -Turned on M56_REV_B24 BOMOPTION

12-01-05: -Added CRITICAL property to 3-pin caps, ESD diodes, and FW chokes
-Added ITPCONN_BOMOPTION
-RC value changes on CPU_Core current sense
-Changed IDE reset pulldown to 15K

EVT

12-01-05: -Changed L4400 to Pb-free part
-Changed J4620 to M8 part
-Added ESD/EMI protection to camera connector
-Removed dual voltage support for trackpad
-Added PM_SOS_STAT_L and PM_SLP_S5_L pulldowns

Revision History

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?
USB2_2CLK	*	25 MIL	DG says

minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

Napa Platform Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	?
FB_CLK	*	=2.5:1_SPACING	?
FB_DATA	*	=2.5:1_SPACING	?

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	?
TMDS	*	=3:1_SPACING	?
VGA	*	15 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	?
TMDS_PAIR2PAIR	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	?
FW	*	=3:1_SPACING	?

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

More System Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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M1 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2,ISL11	0.1 MM	?
1.8:1_SPACING	ISL2,ISL11	0.1 MM	?
2:1_SPACING	ISL2,ISL11	0.1 MM	?
2.5:1_SPACING	ISL2,ISL11	0.1 MM	?
3:1_SPACING	ISL2,ISL11	0.1 MM	?
4:1_SPACING	ISL2,ISL11	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2,ISL11	0.1 MM	?
CLK_PCIE	ISL2,ISL11	0.1 MM	?
CLK_MED	ISL2,ISL11	0.1 MM	?
CLK_SLOW	ISL2,ISL11	0.1 MM	?
CPU_COMP	ISL2,ISL11	0.1 MM	?
CPU_GTLREF	ISL2,ISL11	0.1 MM	?
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	?
DMI	ISL2,ISL11	0.1 MM	?
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
MEM_2OTHER	ISL2,ISL11	0.1 MM	?
PCIE	ISL2,ISL11	0.1 MM	?
SATA	ISL2,ISL11	0.1 MM	?
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	?
VGA	ISL2,ISL11	0.1 MM	?

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	? OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	? OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	? OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	? OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M1 Spacing & Physical Constraints

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	5 7 11 12
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	5 7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	5 7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	5 7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	5 14 23 60
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	5 60
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 86
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 86
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 60
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 60
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	60
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	60

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

	AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
	AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 47
	AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
	AUDIO_55S	AUDIO	ACZ_SYNC	5 21 47
	AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
	AUDIO_55S	AUDIO	ACZ_RST_L	5 21 47
	AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 47
	AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
	AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 47

	TMDS	TMDS	TMDS_CLK_P	77 78 79
	TMDS	TMDS	TMDS_CLK_N	77 78 79
	TMDS	TMDS	TMDS_DATA_P<5..3>	78
	TMDS	TMDS	TMDS_DATA_N<5..3>	78
LV0	TMDS	TMDS	TMDS_DATA_P<2..0>	78
LV1	TMDS	TMDS	TMDS_DATA_N<2..0>	78
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P	79
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N	79
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	
LV2	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	
LV3	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	

M1 Net Properties

SYNC_MASTER=M1_MLB SYNC_DATE=02/10/2006

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